A10B50M-XF180



10-bit, 50 MSPS Analog to Digital Converter IP block

General Description

The A10B50M is an ultra low-power, pipeline analog to digital converter (ADC) intellectual property (IP) design block. It has 10-bit resolution and a sampling rate of up to 50 megasamples per second (MSPS).

The A10B50M maintains its high performance while consuming an exceptionally low power of only 8 mW, making it an outstanding solution for high efficiency designs and applications.

The cost-effective IP block has been designed in a 180 nm CMOS process.

Available as IP and Integrated Circuit.

Key Features

- ♦ 10 bit resolution
- ♦ 50 MSPS sampling rate
- ♦ 8 mW power
- ♦ 50 MHz Input Bandwidth
- ◆ Dynamic Performance:
 - ♦ SFDR: 67 dBc
 - ♦ ENOB: 9.1
- ♦ Hard IP block
- ♦ X-Fab 180 nm process
- ♦ Silicon-validated
- ◆ Radiation-tolerant design available: A10B50MRH

Applications

- ◆ Battery Powered Instruments
- ♦ Sensor/Detector Readout
- Imaging Applications
 - ♦ Image Sensor Readout
 - ♦ Infrared FPA Readout
 - ♦ Medical Imaging

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