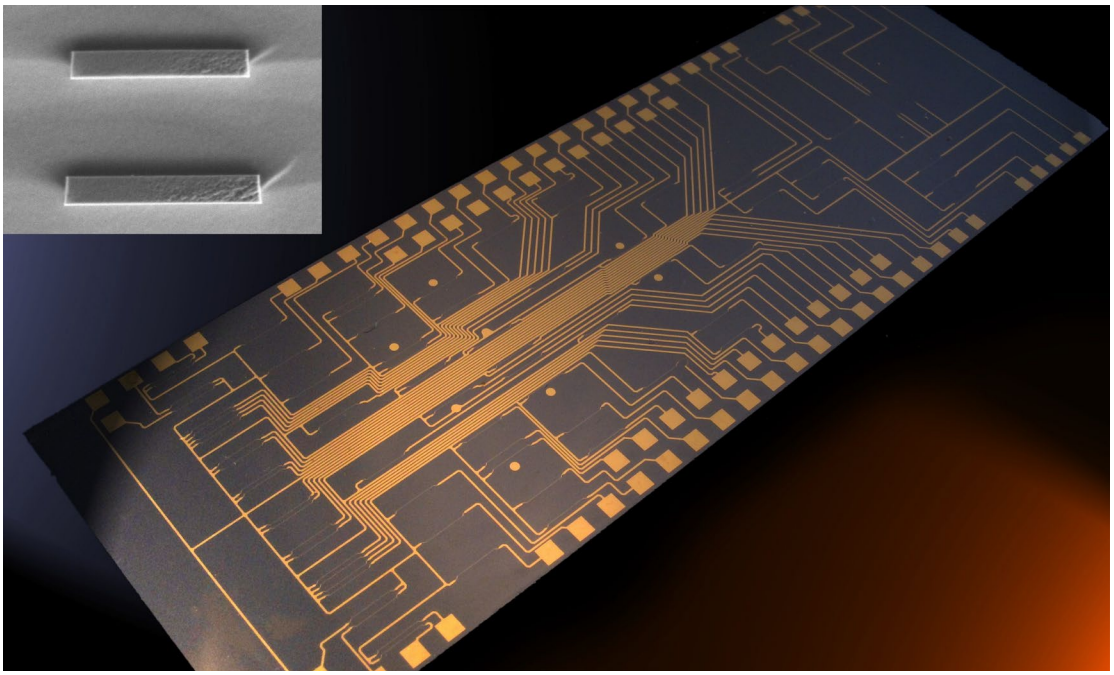
Platform TriPleX™ ADS
MPW run 22: High Contrast

Design Manual



www.lionix-international.com
www.phoenixbv.com

Platform TriPleX™ ADS, Design Manual High Contrast

Disclosure

The information within this document is provided “as is” and no guarantee or warranty is given that the information is fit for any particular purpose. The users use the information at their sole risk and liability.

November 2020.

Table of Contents

Multiple Project Wafer Run using TriPleX™ ADS technology

1 Introduction

In the last years the proprietary TriPleX™ waveguide technology [1] of LioniX International has been further developed and has become one of the three main integrated optical platforms in the Netherlands besides InP and SOI [2]. TriPleX™ structures are realized with CMOS compatible fabrication equipment and the materials used are based on chemical endproducts of LPCVD processes, resulting in very reproducible material properties, allowing design by geometry. The basic concept of a TriPleX™ waveguide consists of a multilayer stack of stochiometric silicon nitride and silicon oxide. These materials have an opposite stress when deposited on a silicon wafer, in which nitride is tensile and oxide is compressive, and stacking them in a multilayer results in a macroscopically low stress layer stack. A basic cross-section of the TriPleX™ waveguide is shown below in figure 1.

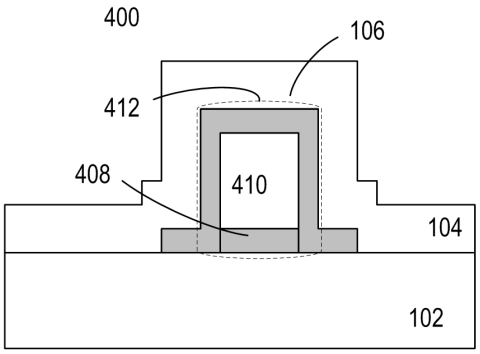


Figure 1. Cross-section of a typical waveguide structure with LPCVD Si3N4 (grey) as basic waveguiding layer, filled in and encapsulated by SiO2 (white). Figure extracted from [3]

Within several projects LioniX International is developing their TriPleX™ waveguide technology into a mature and stable technology platform. In the past several publications have been issued in which the technology and its performance are described in more detail and a few examples are [1][4][7][9]. A good review article from 2015 to start with is [10].

In order to make the TriPleX™ platform more mature and make product development in this technology possible, easy accessibility for customers should be ensured. Other technology platforms make their technology accessible via Multi Project Wafer runs (MPW) and this infrastructure should also be developed for the TriPleX™ technology. LioniX International therefore launches a TriPleX™ MPW. In this call we invite customers seeking for a low cost solution for realizing devices using integrated optics. Our aim is to bring together a number of companies to join in with their custom design on our production of optical TriPleX™ waveguides on 4” wafers thereby reducing the development cost.

In 2011 and 2012, two MPW runs have been carried out based on the low-contrast box-shaped TriPleX™ waveguide. Since then, a new type of waveguide is used based on a high-contrast double-stripe geometry.

2 Specifications

The TriPleX™ ADS waveguides offered within this MPW are designed to operate at the telecom wavelength (1.55 µm) with a **high modal birefringence**. In addition, these waveguides show **a low propagation loss**. The waveguide geometry is chosen such that coupling to and from commercially available optical fibers experiences only a low loss by the **integration of spot size converters** and **Laser building block**.

The waveguides consist of a "double-stripe" shown in TriPleX™ BB using layers of Si_3N_4 with a high refractive index. Furthermore, the cladding and core region consist of SiO_2. The complete waveguide is realized on 100 mm silicon wafers with 8 µm thermal oxide. By tuning the aspect ratio of the box-shape the birefringence can be tailored and minimized.

The optical indices of the single-mode TriPleX™ waveguides are summarized in the following table for TE polarization only. TM polarization can also propagate but with much larger propagation loss and bending loss and is therefore not supported:

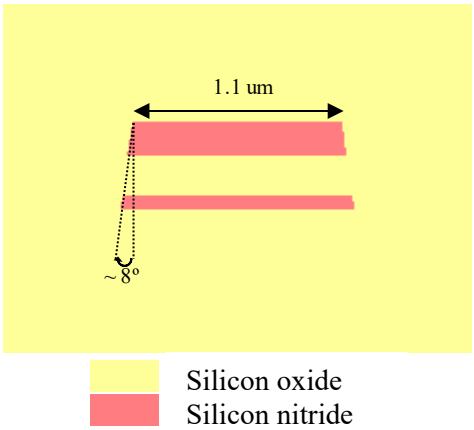


Figure 2. Cross-section of the TriPleX™ ADS waveguide in Si3N4 with SiO2 cladding.

Table 1. Effective indices of TriPleX™ ADS waveguide. Specs are given at a wavelength of 1.55 µm and a waveguide width of 1.1 µm.

Optical Property @ λ = 1.55 µm	**TE_{00}**
Effective index of the mode	1.530 ± 0.005
Group index of the mode (indication)	~ 1.77
Channel birefringence of a straight waveguide	> 10^{-2}
Straight waveguide loss	≤ 0.5 dB/cm

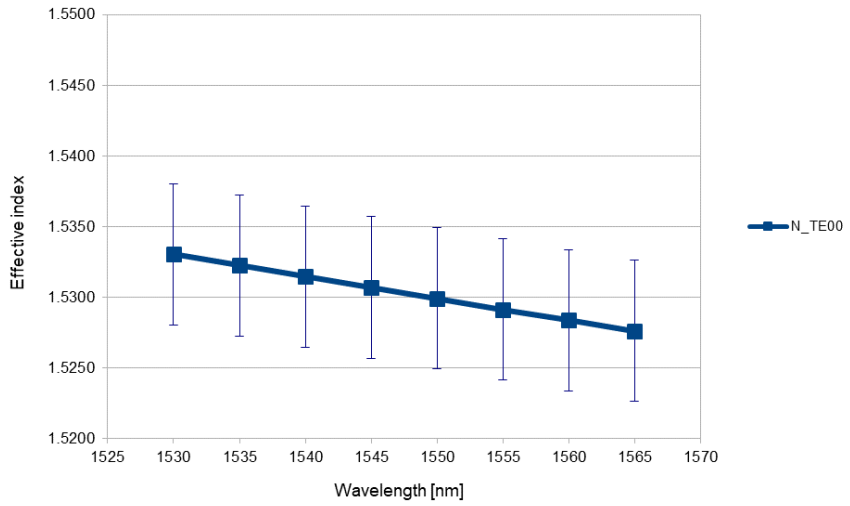


Figure 3a. Effective index as a function of wavelength for the TE_{00} mode of a straight TriPleX™ ADS waveguide (single-mode, width 1.1 µm).

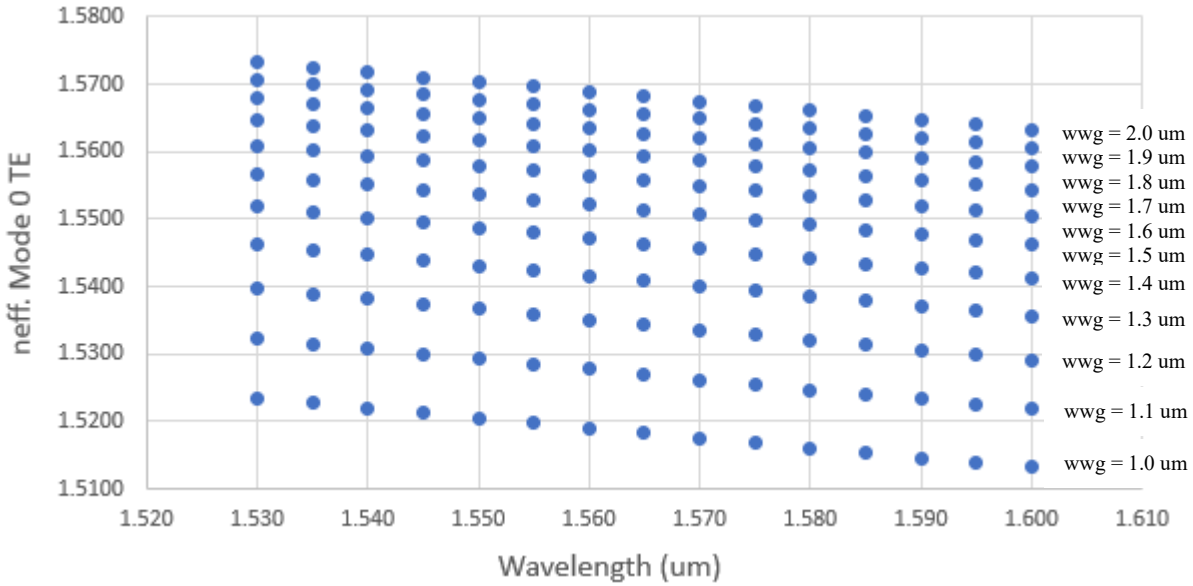


Figure 4b. Effective index as a function of wavelength for the TE_{00} mode of a straight TriPleX™ ADS waveguide. Waveguide width (wwg) range from 1.0 um until 2.0 um.

3 Fiber-chip coupling

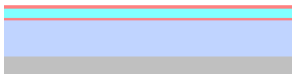
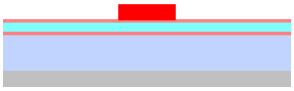
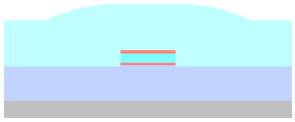
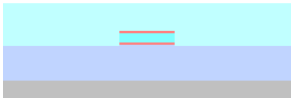
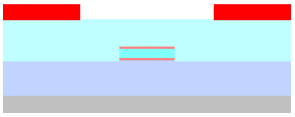
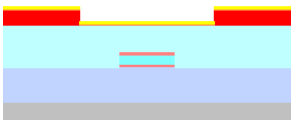
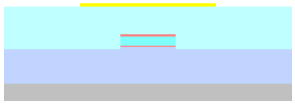
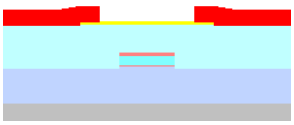
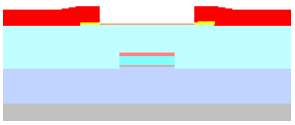
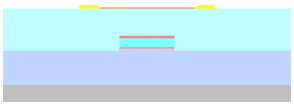
To be able to improve the fiber-to-chip coupling efficiency, both silicon nitride layers will be made with spot-size converters at the chip facets for the in- and output waveguides. The on-chip waveguide with a default width of 1.1 µm has mode field diameter (MFD) of appr. 1.7 µm at telecom wavelength. To match the MFD of the waveguides at the chip facet, locally the silicon nitride is vertically tapered down during production. The MFD of this spot-size converter is appr. 10 µm at telecom wavelength, which is matched to that of the standard telecom fiber (SMF28).

For post manufacturing assembly there is a design manual which should be taken into account already at the beginning of the design phase. This design manual is added as appendix 1 to this manual.

4 Manufacturing

The process flow of the manufacturing of the TriPleX™ waveguides with chromium heaters and leads of a stack of chromium and gold is given in Table 2, step by step.

Table 2. Process flow (cross-section) of the TriPleX™ waveguides with heaters of chromium and leads of chromium+gold

 1) Silicon substrate	 2) Thermal oxidation silicon substrate	 3) LPCVD Si_3N_4 deposition (1)	 4) LPCVD TEOS SiO_2 deposition
 5) LPCVD Si_3N_4 deposition (2)	 6) Lithography waveguide mask	 7) Dry etch waveguide	 8) Removal of the resist
 9) PECVD SiO_2 deposition	 10) Chemical mechanical planarisation	 11) Lithography lead mask	 12) Cr/Au deposition
 13) Lift-off of the metal stack by resist removal	 14) Lithography heater mask	 15) Wet etch Au	 16) Removal of the resist

The heater definition is a good example of the difference between cross-section and mask layers in the PhoeniX software, which can be illustrated by the following script lines:

```
mask::CScreate("mcsHEATER",filter,clr_green,1,0);
mask::AddGrid(msk_Lead,1e-2);
mask::AddGrid(msk_Heater,1e-2,,{w->w+10});
mask::CScreate("mcsLEAD",filter,clr_blue,1,0);
mask::AddGrid(msk_Lead,1e-2);
```

In this way, both the lead mask (msk_Lead) and the heater mask (msk_Heater) are added to the cross-section mcsHEATER. The argument {w->w+10} in the third line specifies that all structures in msk_Heater have to become 10 µm wider than specified for the structures in msk_Lead mask. This is to be sure that all gold will be etched away from the regions where the heaters are defined.

5 Wafer map and dicing

The 100 mm diameter silicon wafer is divided into a matrix of 4 x 4 blocks of 16 mm x 16 mm, as indicated in Figure 4. Per participant, a maximum of two blocks will be assigned (depending on required space for their design).

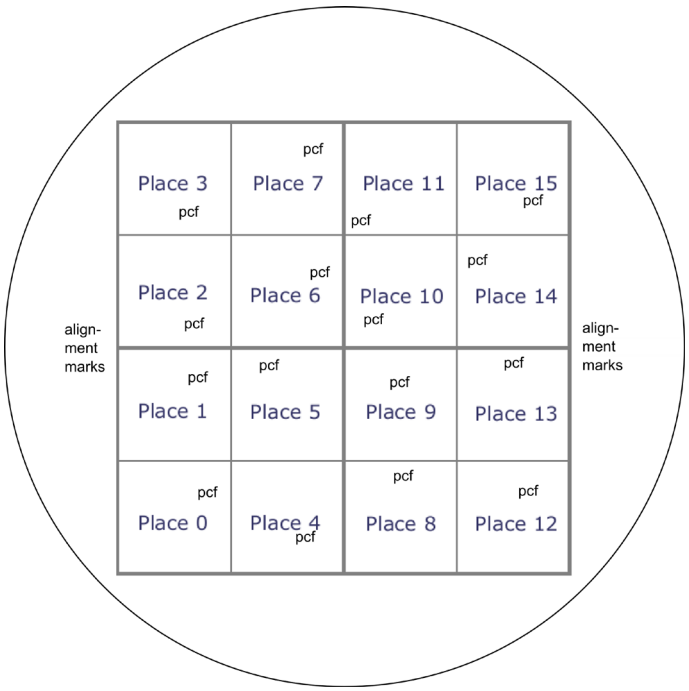


Figure 5. Wafer map showing the place of the blocks on the wafer; outside the blocks alignment marks will be added, inside each block, a process control features set (pcf) will be placed on a suitable place.

In each of the blocks a Process Control Feature will be added to control the dimensions of the waveguides. LioniX International will verify the width of the waveguide by measuring the PCF on several positions on the wafer. The functional performance of the waveguides will be verified by LioniX International on an additional set of testdevices on the wafer. Additional measurements on specific dimensions in the design of the users will not be a part of this MPW. In case users would really need a dimension to be verified this can be done at additional cost.

The placement of the blocks will influence the dicing scheme. The allocated room for dice lines is 300 µm. This is based on the width of the dicing blade suitable for dicing glass. For pigtailing, it is necessary to glue glass on top of the dies. In the current MPW run, no pigtailing is included; this can be ordered at additional cost at LioniX International. The silicon wafer will be diced using a dicing blade suitable for dicing silicon, having a width of 30 µm. This means that the exact die size will be 135 µm larger on all sides. For this reason, waveguides at the facets should be defined until half the dice line width.

The dice lines on the masks will be 15 µm wide, so that after dicing, they are completely removed by dicing.

5.1 Diceline definition

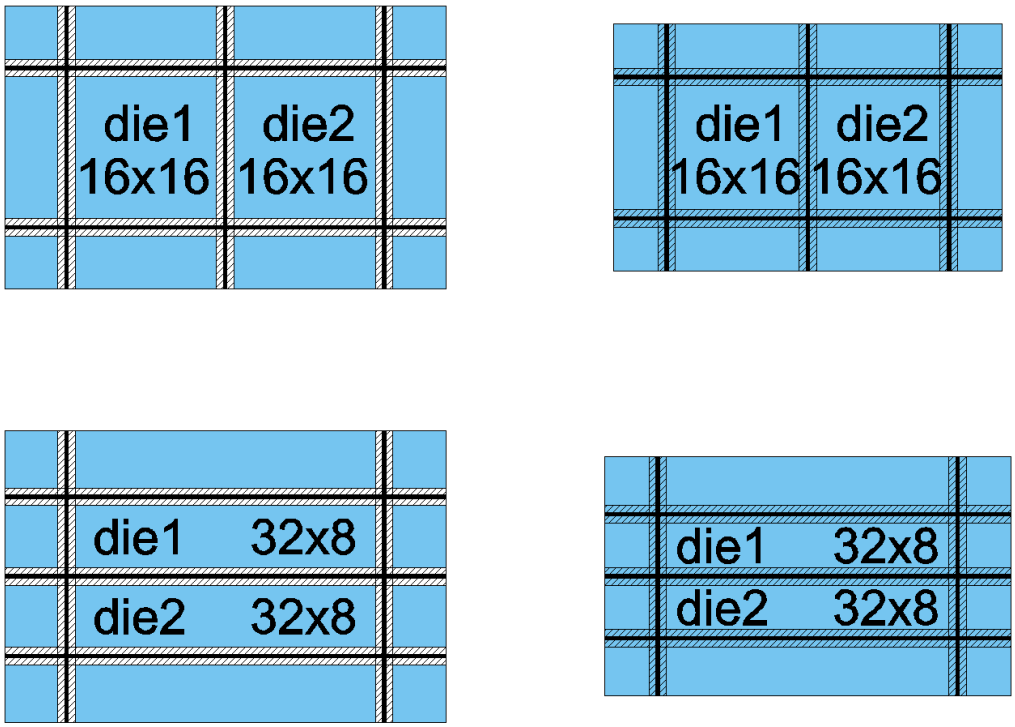


Figure 6. Before dicing: left column: the old definition ("exclusive dicelines"), right column: the new definition ("inclusive dicelines"); top row: 16×16 tiles, bottom row: 32×tiles.

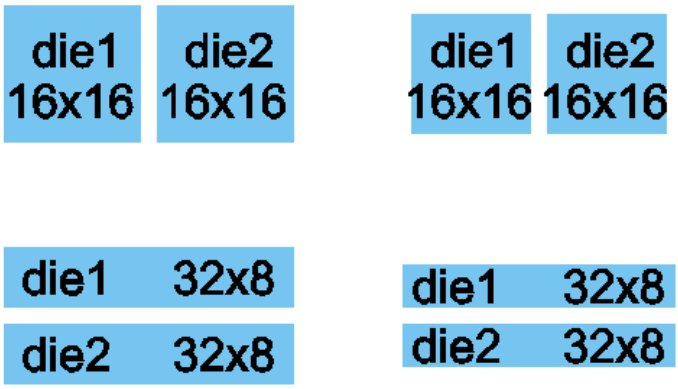


Figure 7. After dicing: left column: the old definition ("exclusive dicelines"), right column: the new definition ("inclusive dicelines"); top row: 16×16 tiles, bottom row: 32×tiles.

Table 3. Dimensions of the design area and pitches of the dicelines, of the old and new diceline definition.

Diceline Definition	old (until MPW12)		new (from MPW13)	
	16×16	32×8	16×16	32×8
Design Area				
length [µm]	16,000	32,300	16,000	32,000
width [µm]	16,000	7,850	16,000	8,000
Dicing Pitches				
horizontal [µm]	16,300	32,600	16,000	32,000
vertical [µm]	16,300	8,150	16,000	8,000

6 Design rules

First the global design rules are given. In the next Section, for each building block the free parameters and their ranges and default values are given.

Optical waveguides:

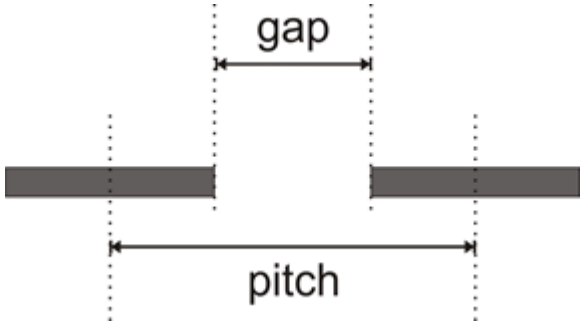


Figure 8. Definition of pitch and gap (cross-section).

Figure 9. Definition of pitch and gap (topview).

1. Minimum waveguide width: 1.0 µm (defined at the top of the nitride core, see also Figure 2);
2. Minimum radius of curvature: 80 µm (negligible bend loss for TE only);
3. Mininum gap between optical waveguides: 1.0 µm.

The definition of the gap is the distance between the top of the waveguides. This also applies to the definition of the pitch and the waveguide width. Please see Figs 7 and 8.

Electrical parts:

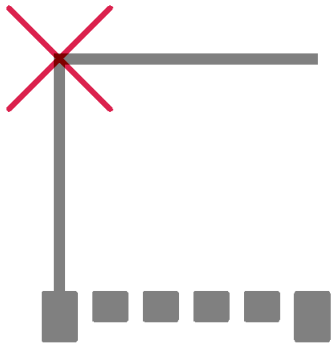


Figure 10. A sharp corner can lead to defective leads.

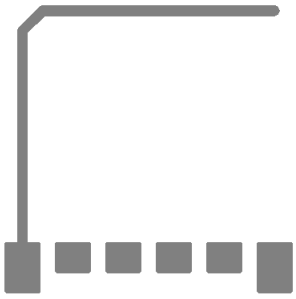


Figure 11. Better use wires and angles of 135°.

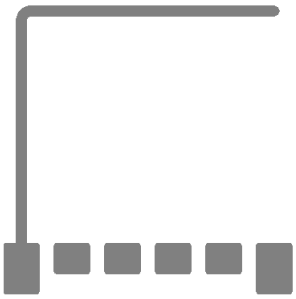


Figure 12. Or equivalently, use bends of 90°.

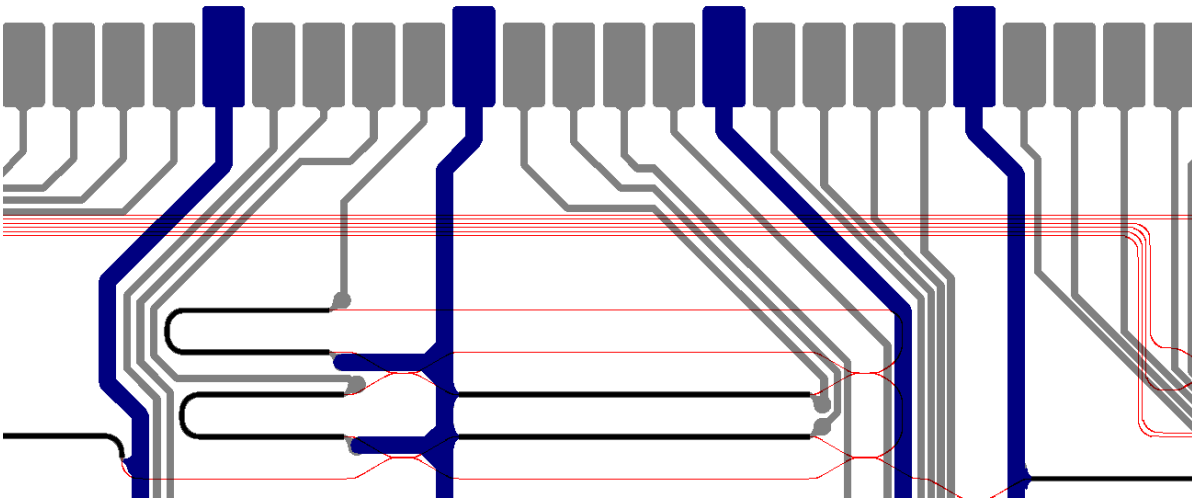


Figure 13. Example (not designed in the TriPleX IR MPW PDK) of routing between heaters (■) and contact pads: each heater has to be connected to a signal pad (■) and a ground pad (■).

4. Heater width: 20 µm; Lead width: if possible, 100 µm is preferred. If this does not work, you can go down to 40 µm. However, even then, try to make the ground leads 100 µm wide;
5. Avoid sharp corners, especially at the inside of corners (by using rounded shapes, or in case of straight wires, use angles of e.g. 135 degrees, see Figs. 9, 10 and 11);
6. Minimum gap between electrical parts: 30.0 µm;
7. Multiple heaters may be connected to the same ground pad.

However, if one want to use the Characterisation Packaging Service (See Appendix 1), it is not allowed to connect both sides of a heater to ground pads. The reason for this is that on the standard carrier PCB, all grounds are electrically connected with each other (see Fig. 12).

Thermo-optic modulation:

8. Minimum pitch between a heater and an adjacent waveguide: 250 µm (for a thermal crosstalk of -17 dB);

General:

9. Do not place structures too close to the chip edges (with the exception for the input and output waveguides, that have to be there); stay away at least 250 µm from the edge of the design area, because of a) chipping of small fragments might ruin them, b) to have enough room to accommodate half the width of the widest dicing blade (which is ≤150 µm) and for polishing.

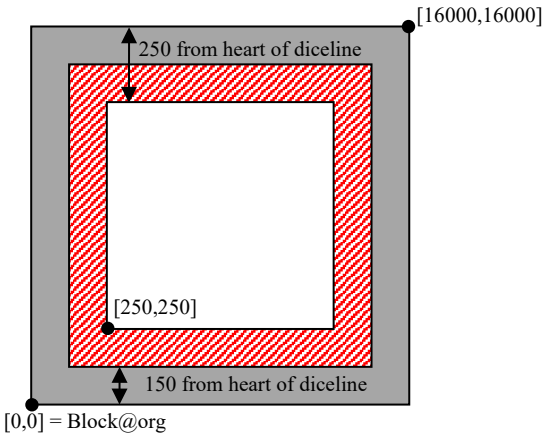


Figure 14. The new design area due to the new diceline definition: ▭ = half the (maximum) diceline width of 150 µm, ▭ + ▨ = waveguide keep-out region, ▭ = design area.

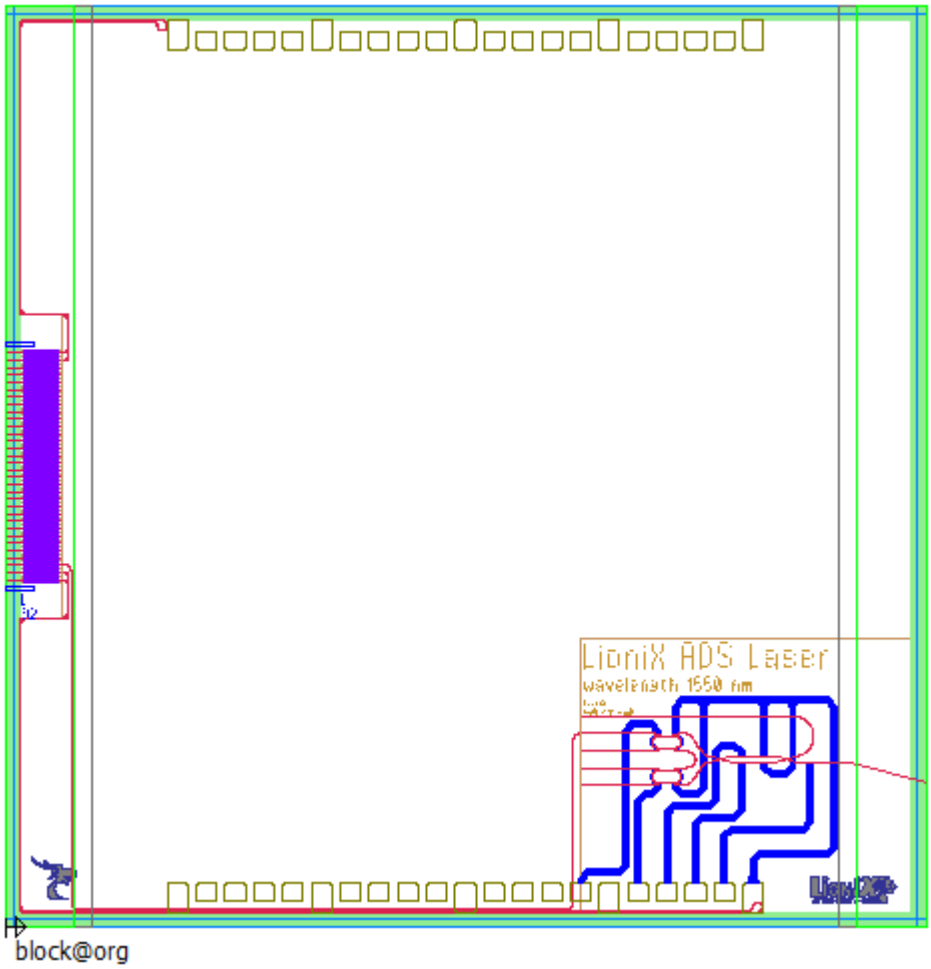
Since MPW13, A new diceline definition is in use (see also Section 5.1 and Fig. 13). The coordinates of the corners of the design area for the 16×16 die are still at [0,0] = Block@org and [16000,16000]. However, instead of placing the dicelines outside of the design area, they are now for 50% inside the design area. In practice one does not have to consider explicitely the exact diceline widths, as they are taken care of because of the waveguide keep-out region defined by Design Rule 9. In case one would like to know the exact chip dimensions are after the chips have been made suitable for pigtailing and packaging using the Charactersation Packaging Service, please contact Lionix International.

A note, especially to previous users of the TriPleX IR MPW:
Now the reference point Block@org is in the keep-out region for waveguides, meaning that one cannot place an optical component on this position; because of Design Rule 9, the closest point that can be used is at [250,250], see also Fig. 13.

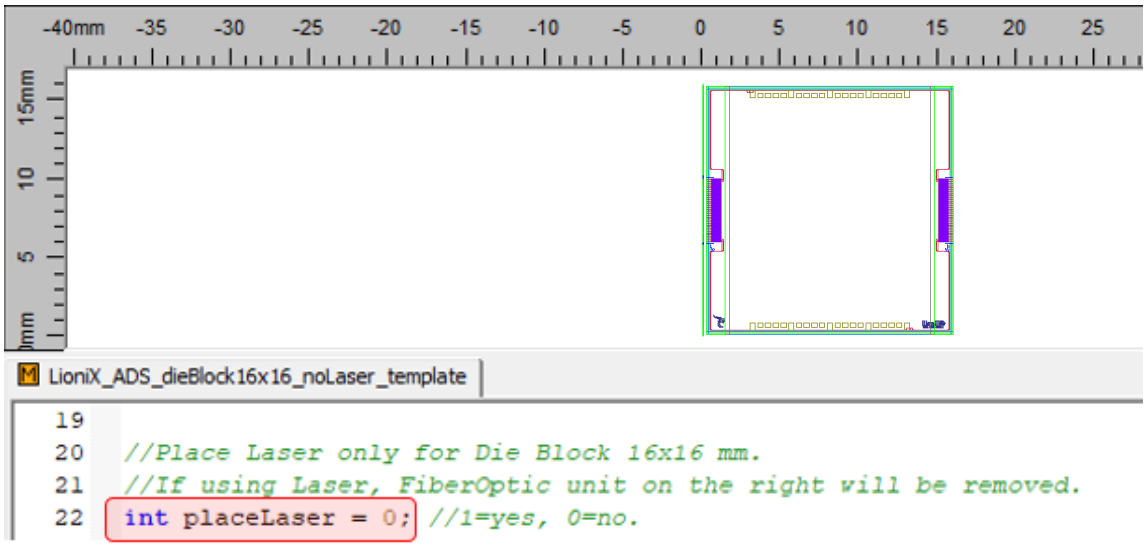
7 Die template

7.1 Die template 16x16

Die template name: Lionix_ADS_DieBB16x16	**Disclosure:** Public
Version: 1.0.0	**License:** Triplex Library
Replaces: None	**ReplacedBy:** None
Description: Die template for a die of 16 mm × 16 mm, suitable for standard packaging on a PCB or for manual placement of probe pens. This die template is also suitable for integration with the laser building block. The fiber array is on the left, and the connection to the laser is on the bottom right. If the laser building block is not used, there can be two fiber arrays (left, right). There can be two DC pad arrays (top, bottom). Here, adapter type "pC" has been selected for both bondpad arrays, which has 20 bondpads (see Appendix, Table 2.4 for more information).	



Parameters:	**Rangespec:**
placeLaser: if the parameter is set to one, the Laser building block is going to be placed correctly in the die template. If the parameter **placeLaser** is set to zero (hence, the Laser building block is not used), then the FiberOptic unit on the right can be placed by using the parameter amount_FiberOptic_Right.	[**1**=Yes, 0=No]



LionIX_ADS_dieBlock16x16_noLaser_template

```
19
20  //Place Laser only for Die Block 16x16 mm.
21  //If using Laser, FiberOptic unit on the right will be removed.
22  int placeLaser = 0; //1=yes, 0=no.
```

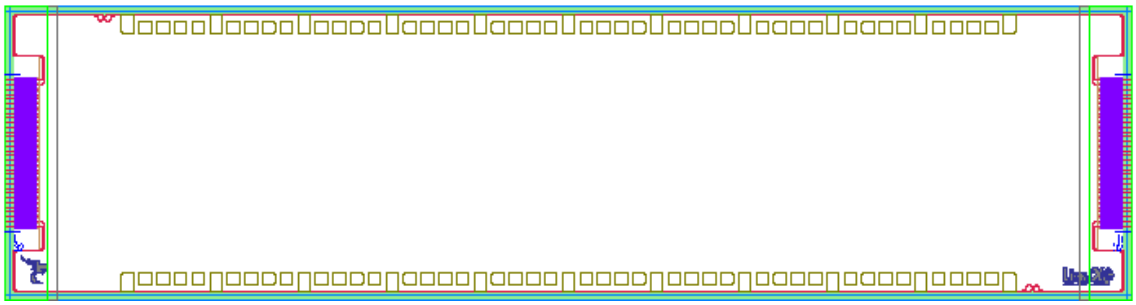
Parameters:

amount_FiberOptic_Left: set Fiber Array Unit (FAU) on the left.	[0,8,12,16,24,28,32]
amount_FiberOptic_Right: set the FAU on the right.	[0,8,12,16,24,28,32]
Alignment: types of the alignment waveguides, please see Table 4 below. Alignment = 0 does not need FAU. Alignment = 4 needs both FAU on the left and on the right.	[0,**4**]
DCPad_type: BondPad is suitable for standard packaging on a PCB, ProbePad is suitable for manual placement of probe pens.	[**BondPad**, ProbePad]
amount_BondPad_top	[0,**20**]
amount_BondPad_bottom	[0,**20**]
adapterTypeTop	[**"pC"**]
adapterTypeBottom	[**"pC"**]

Optical ports: block@out0,...,out(N-1) If using the Laser building block: laser@out0	**DC ports:** block@dc0,...,dc(M-1)

7.2 Die template 32x8

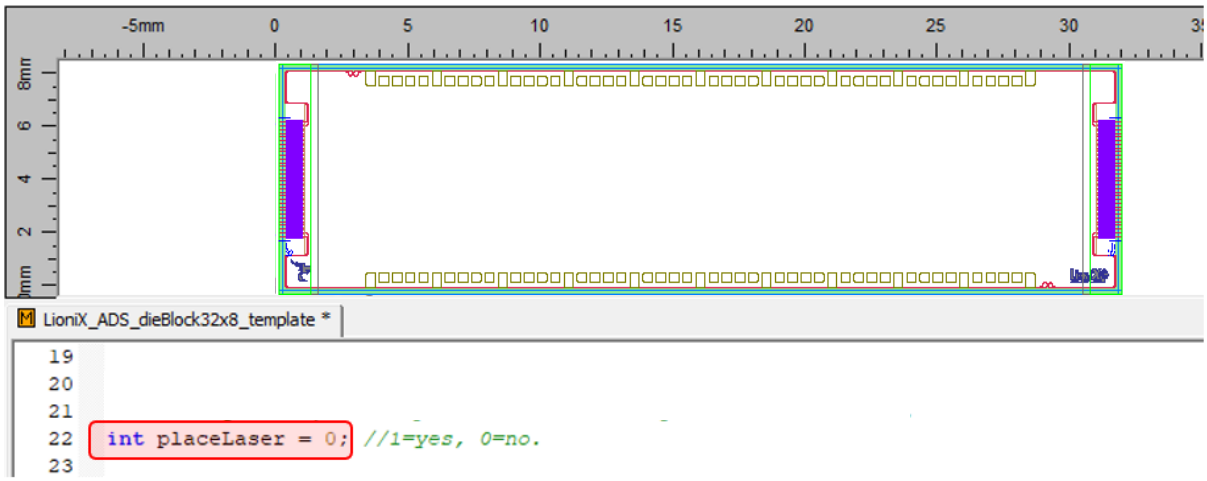
Die template name: lionixDieBB32x8	**Disclosure:** Public
Version: 1.0.0	**License:** Triplex Library
Replaces: None	**ReplacedBy:** None
Description: Die template for a die of 32 mm × 8 mm, suitable for standard packaging on a PCB or for manual placement of probe pens. There can be two fiber arrays (left, right) and two DC pad arrays (top, bottom). Here, adapter type "pD" has been selected for both bondpad arrays, which has 50 bondpads (see Appendix, Table 2.4 for more information). To use this die template, set the die parameter placeLaser = 0.	



Parameters: **NOTE:** set parameter **placeLaser =0**.	**Rangespec:** [0]
amount_FiberOptic_Left: set Fiber Array Unit (FAU) on the left.	[0,8,12,16,24,28,32]
amount_FiberOptic_Right: set the FAU on the right.	[0,8,12,16,24,28,32]
Alignment: types of the alignment waveguides, please see Table 4 below. Alignment = 0 does not need FAU. Alignment = 4 needs both FAU on the left and on the right.	[0,**4**]
DCPad_type: BondPad is suitable for standard packaging on a PCB, ProbePad is suitable for manual placement of probe pens.	[**BondPad**, ProbePad]
amount_BondPad_top	[0,20,**50**]
amount_BondPad_bottom	[0,20,**50**]
adapterTypeTop	["pC", **"pD"**]
adapterTypeBottom	["pC", **"pD"**]
NOTE: adapterType: "pC" sets 20 BondPads. "pD" sets 50 BondPads.	

Optical ports: block@out0,...,out(N-1)	**DC ports:** block@dc0,...,dc(M-1)

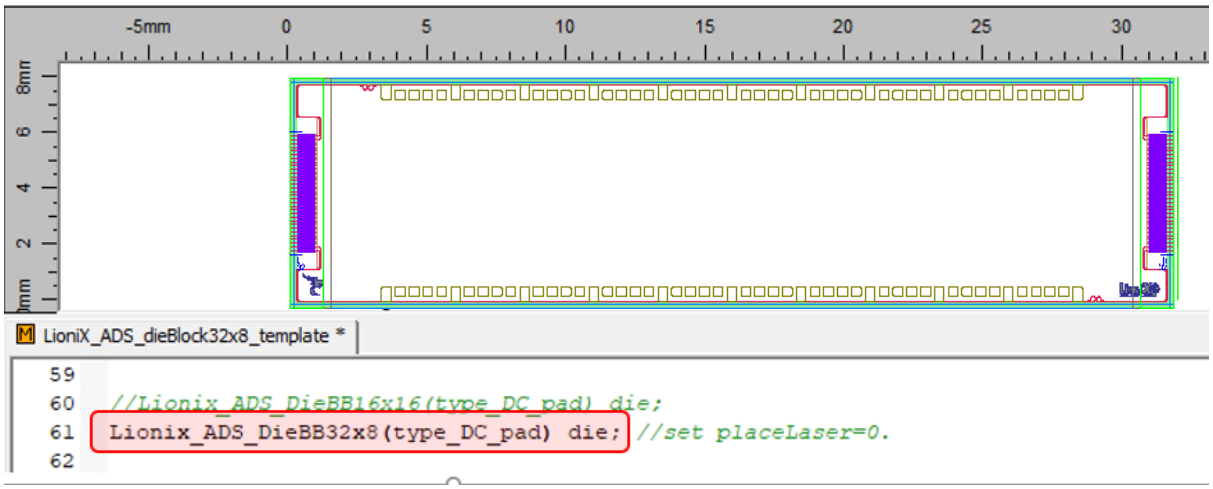
Screenshots below show how to get the die template 32x8 mm :



Afterward, please uncomment the script:

LioniX_ADS_DieBB32x8(type_DC_pad) die;

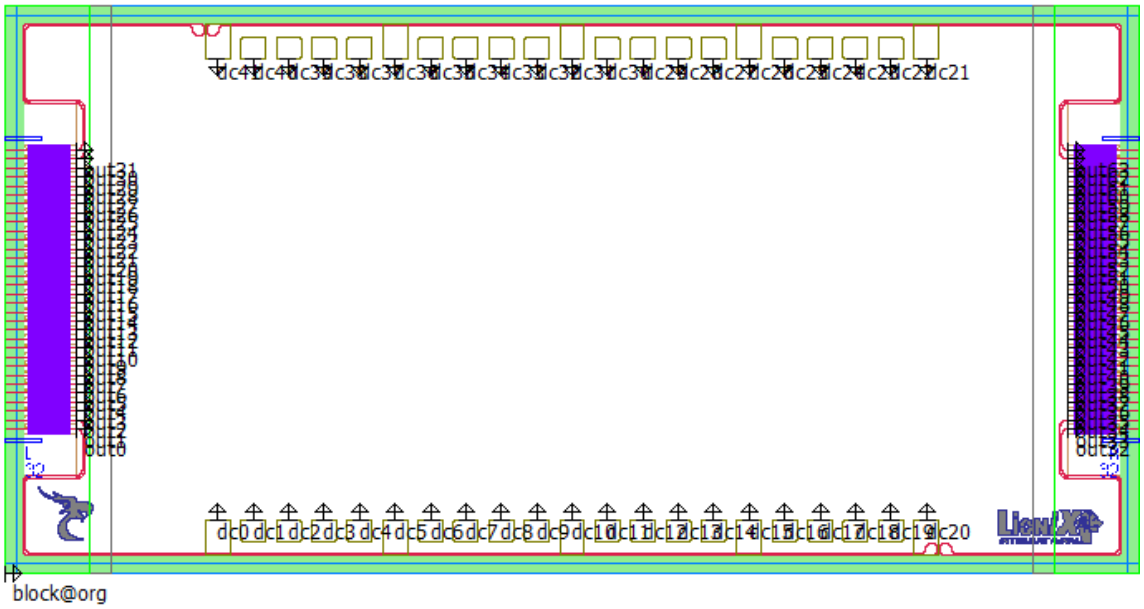
This is shown in the screenshot below:



7.3 Die template 16x8

Die template name: lionixDieBB16x8	**Disclosure:** Public
Version: 1.0.0	**License:** Triplex Library
Replaces: None	**ReplacedBy:** None

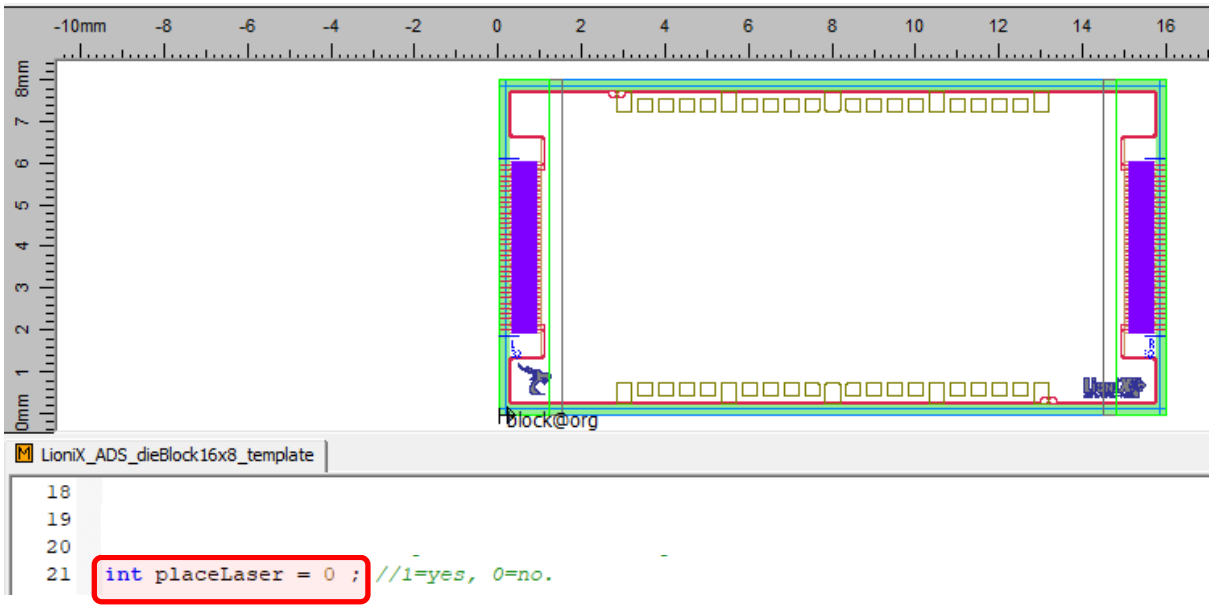
Description: Die template for a die of 16 mm × 8 mm, suitable for standard packaging on a PCB or for manual placement of probe pens. There can be two fiber arrays (left, right) and two DC pad arrays (top, bottom). Here, adapter type "pC" has been selected for both bondpad arrays, which has 20 bondpads (see Appendix, Table 2.4 for more information). To use this die template, set the die parameter placeLaser = 0.



Parameters: **NOTE:** set parameter **placeLaser =0**.	**Rangespec:** [0]
amount_FiberOptic_Left: set Fiber Array Unit (FAU) on the left.	[0,8,12,16,24,28,32]
amount_FiberOptic_Right: set the FAU on the right.	[0,8,12,16,24,28,32]
Alignment: types of the alignment waveguides, please see Table 4 below. Alignment = 0 does not need FAU. Alignment = 4 needs both FAU on the left and on the right.	[0,**4**]
DCPad_type: BondPad is suitable for standard packaging on a PCB, ProbePad is suitable for manual placement of probe pens.	[**BondPad**, ProbePad]
amount_BondPad_top	[0,**20**]
amount_BondPad_bottom	[0,**20**]
adapterTypeTop	[**"pC"**]
adapterTypeBottom	[**"pC"**]

Optical ports: block@out0,...,out(N-1)	**DC ports:** block@dc0,...,dc(M-1)

Screenshots below show how to get the die template 16x8 mm :



Afterward, please uncomment the script:

LioniX_ADS_DieBB16x8(type_DC_pad) die;

This is shown in the screenshot below:

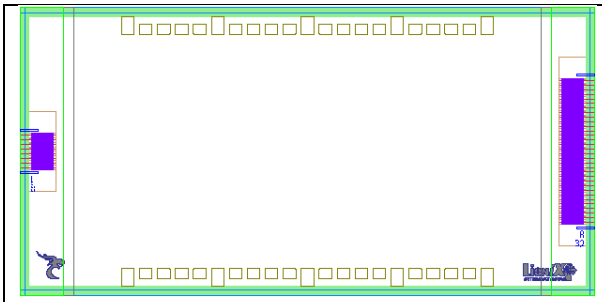
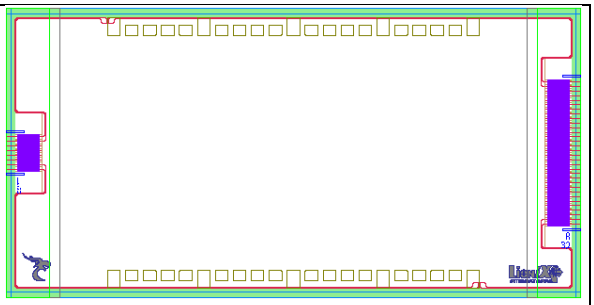
For pigtailing, one can define different types of alignment waveguides (see also Appendix 1, Chapter "PIC design rules for fiber array pigtailing").

To finetune the amount of fibers and DC pads, one can modify the following code in the Lionix template script just before the line of the command for invoking the lionixDieBB:

```
int amount_FiberOptic_Left  = 8;      // allowed values: 0, 8, 12, 16, 24, 28, or 32
int amount_FiberOptic_Right = 16;     // allowed values: 0, 8, 12, 16, 24, 28, or 32
int AlignmentWG = 4;                  // 0=no alignment waveguides. 4=four alignment loop waveguides.
//Lionix_ADS_DieBB16x16 (type_DC_pad) die;
```

Table 4 shows how the different options for the alignment waveguides look like.

Table 4. The different options of the variable AlignmentWG.

 AlignmentWG = 0: no alignment waveguides, not suitable for pigtailing of fiber arrays.	 AlignmentWG = 4: four alignment loop waveguides

8 Building blocks

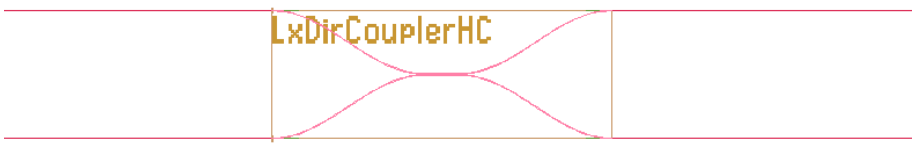
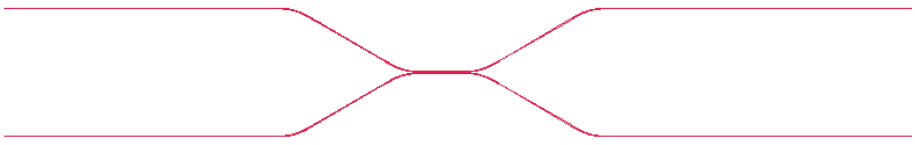
The building blocks and their adjus parameters are given below. In **Rangespec** the range in which parameters can be varied is given in the format:

[a, **b**, c]
a = minimal value
b = default value (bold)
c = maximum value (all values in µm)

To exclude a single specific value d from the range, the following notation is used: [a, **b**, c]\d
A value of 1.0E6 means that there basically is no maximum (or minimum)
Any component performance specification that is given is always given for the default value and is not valid for other values.

Most building blocks are public. However, there are also private building blocks. In the mask file generated by the PhoeniX software, there will be holes in the waveguide mask design. These holes will be filled in by LioniX International – based on additional files generated by the software – that should be delivered with the design, see also section "Mask file generation". As the contents of these private building blocks are not public, you will not get to see the end result in high resolution. We can also show screen shots or prepare a mask file, in which the private content has been stripped from, so that you are able to judge whether we have properly merged your design in the final mask set. The procedure of how we deal with private building blocks is summarized in Table 5.

Table 5. Procedure for dealing with private building blocks.

a) The MPW participant sees a mockup (pink, mcsWAVEGUIDE_nogds) within a bounding box with the name of the private building block (brown), together with his own design (red) in the viewer of OptoDesigner: 
b) When the participant presses the "Start" button, DRC checks are carried out and a number of files (9 in total) are generated, amongst which a mask file (gds), that contains a hole at the position of the private building block: 
c) After transferring the files to the foundry, LioniX International, an spt file containing the position and parameter information allows a correct insertion of the private mask layout of the foundry (not shared with the participant): 

Modified BBs since MPW10

Starting with MPW10, the BBs and their names have been modified. One BB is not present anymore, viz. the LxJunctionHC: this BB allowed to define a straight-to-bend offset between two given elements. As the bent BBs now automatically take care of this, the LxJunction BB is considered obsolete and has been removed. An overview of the folder structure of the BBs, as implemented in the "Insert Element" dialog in OptoDesigner is presented in Fig. 14.

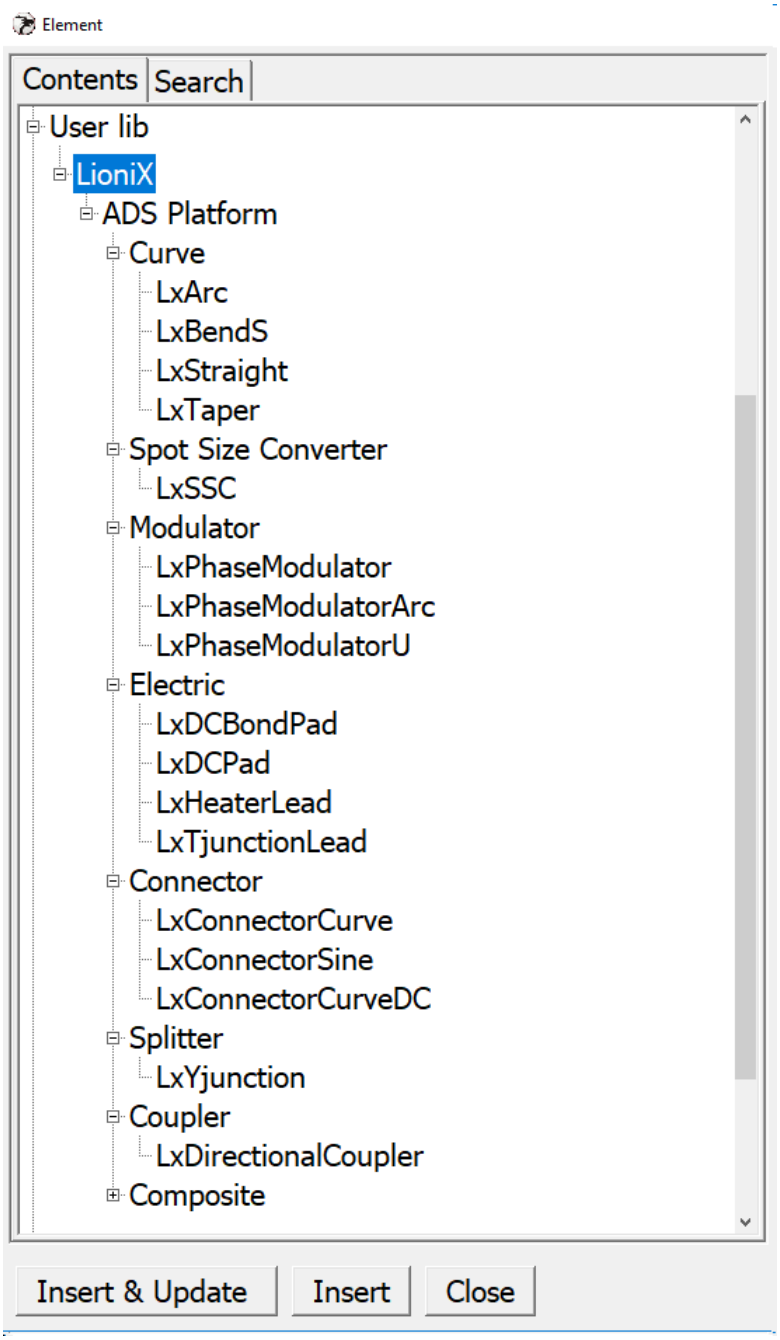


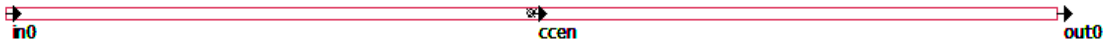
Figure 15. BB folder structure in the "Insert Element" dialog in OptoDesigner.

Please note that the naming of some BBs has been changed, because of harmonization with BB names in PhoeniX PDKs for other foundries. Table 6 lists the currenly used names and old names.

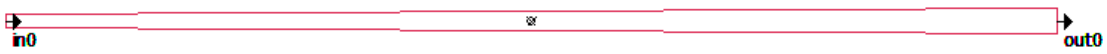
Table 6. Overview of the new LioniX International PDK folder structure and BB names, and the old BB names.

New BB names from MPW10	Old BB names until MPW10
Curve	
LxArc	LxBendHC
LxStraight	LxStraightHC
LxTaper	LxLateralTaperHC
LxBendS	LxBendSHC
Spot Size Converter	
LxSSC	
Electrics	
LxDCpad	
LxHeaterLead	LxHeaterLeadHC
LxDCBondPad	
LxTjunctionLead (new from MPW13)	
Modulator	
LxPhaseModulator	LxTOPM,LxTOPMStraightHC,LxTOMStraightHC
LxPhaseModulatorArc	LxTOMArcHC
LxPhaseModulatorU	
Connector	
LxConnectorCurve	
LxConnectorCurveDC	
LxConnectorSine	
Splitter	
LxYjunction	LxYjuncHC
Coupler	
LxDirectionalCoupler	LxDirCouplerHC
Removed BB	
	LxJunctionHC

BB folder: Curve

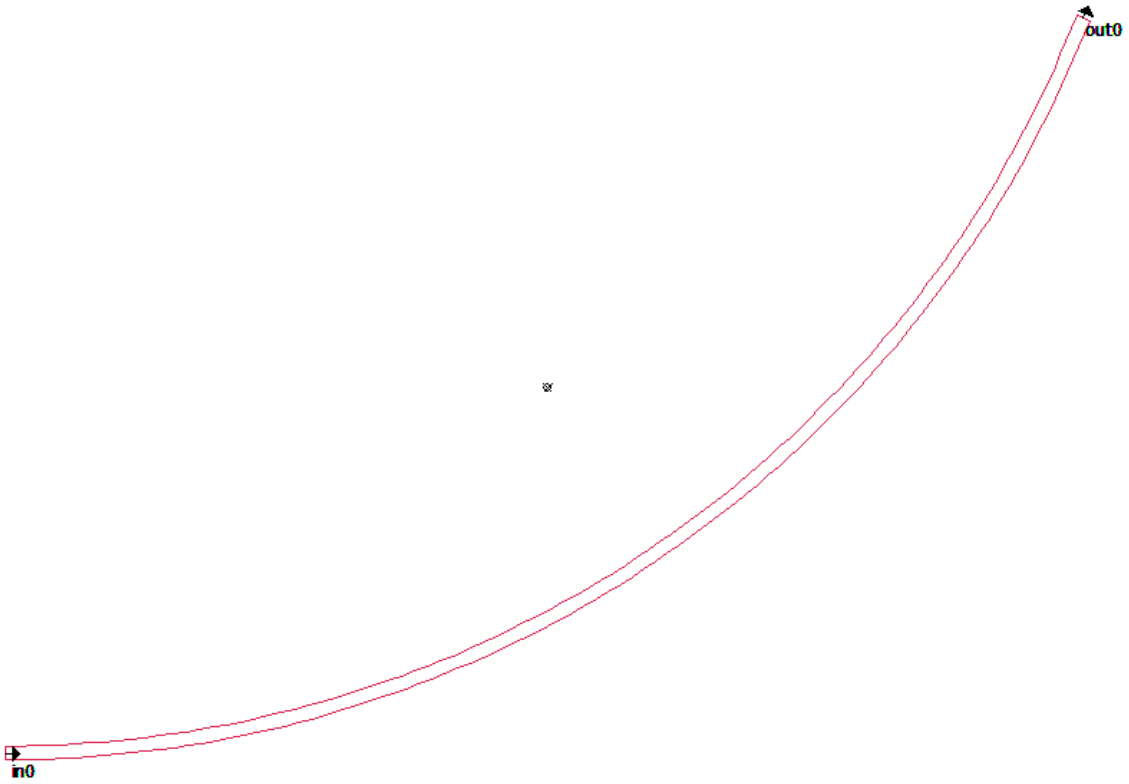
BB name: LxStraight	**Disclosure:** Public
Version: 1.0.2	**License:** Triplex Library
Replaces: LxStraight v1.0.1	**ReplacedBy:** None
Description: A straight optical waveguide with constant width.	
	
Parameters: Length: length of the waveguide Width: width of the waveguide simLoss: assumed propagation loss for circuit simulators [dB/cm]	**Rangespec:** [0.1, **100.0**, 1.0E6] [1.0, **1.1**, 1.0E6] [0.0, **0.5**, 1.0E6]
Optical ports: in0, out0, ccen	**DC ports:** None

BB folder: Curve

BB name: LxTaper	**Disclosure:** Public
Version: 1.0.2	**License:** Triplex Library
Replaces: LxTaper v1.0.1	**ReplacedBy:** None
Description: A straight optical waveguide with linearly varying width.	
	
Parameters: Length: length of the lateral taper WidthIn: input width of the lateral taper WidthOut: output width of lateral. taper simLoss: assumed propagation loss for circuit simulators [dB/cm]	**Rangespec:** [0.1, **100.0**, 1.0E6] [1.0, **1.1**, 1.0E6] [1.0, **2.2**, 1.0E6] [0.0, **0.5**, 1.0E6]
Optical ports: in0, out0	**DC ports:** None

BB folder: Curve

BB name: LxArc	**Disclosure:** Public
Version: 1.0.2	**License:** Triplex Library
Replaces: LxArc v1.0.1	**ReplacedBy:** None
Description: A bent optical waveguide with constant width and radius of curvature. Please note that the location of the optical ports (in0, out0) is not the heart line of the arc, but the position of maximum optical power (to account for a straight-to-bend offset). The built-in straight-to-bend offset (SBoffset) is a function of wavelength, waveguide's width and bend radius, for TE polarization.	

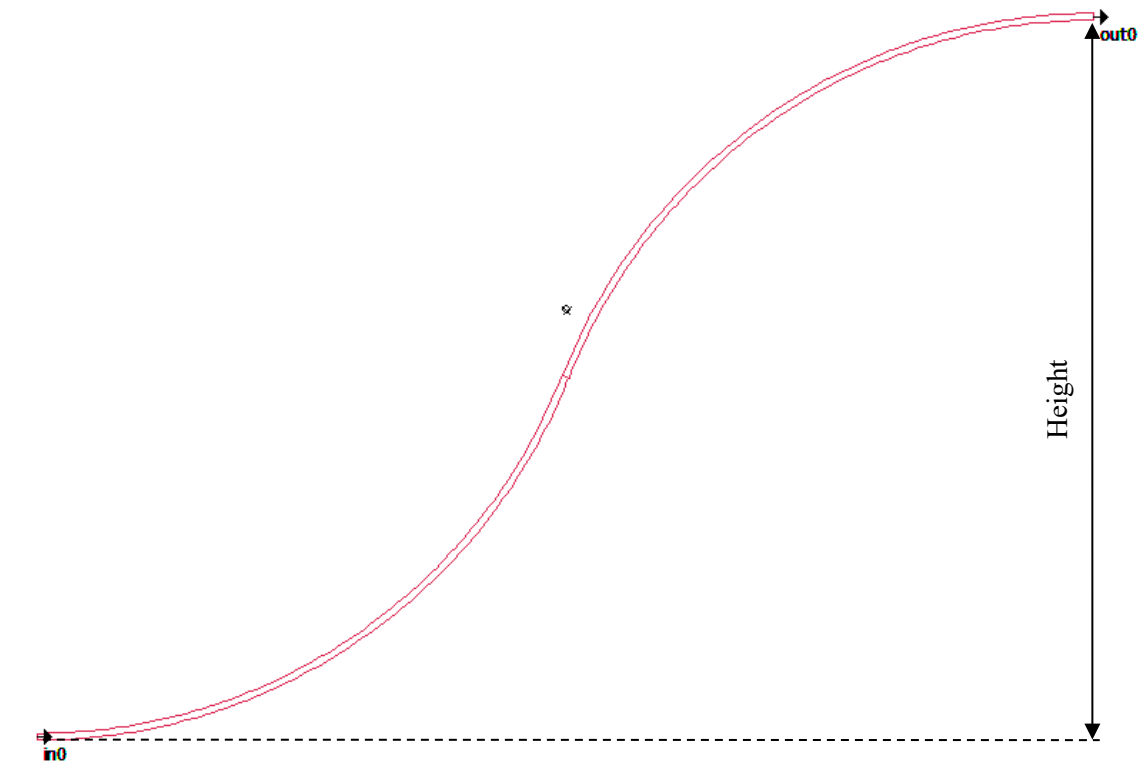


Parameters:	**Rangespec:**
Angle: angle of the bend [°]	[-360.0, **180.0**, 360.0]
Radius: radius of curvature of the bend waveguide [um]	[85.0, **100.0**, 1.0E6]
Width: width of the bend waveguide [um]	[1.0, **1.1**, 1.0E6]
Wavelength [um]	[1.52,**1.55**,1.60]
simLoss: assumed propagation loss for circuit simulators [dB/cm]	[0.0, **0.5**, 1.0E6]

Optical ports: in0, out0	**DC ports:** None

BB folder: Curve

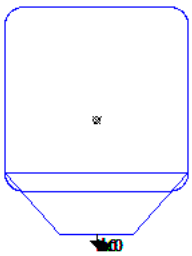
BB name: LxBendS	**Disclosure:** Public
Version: 1.0.2	**License:** Triplex Library
Replaces: LxBendS v1.0.1	**ReplacedBy:** None
Description: An S-shaped bent optical waveguide with constant width and radius of curvature; the waveguide input and output have the same direction. This building block is based on LxArc and therefore also by default takes care of the straight-to-bend offsets (SBoffset). The built-in SBoffset is a function of wavelength, waveguide's width and bend radius, for TE polarization.	



Parameters:	**Rangespec:**
Height: vertical offset of the S-bend	[-1.0E6, **127.0**, 1.0E6]
Radius: radius of curvature of S-bend	[85.0, **100.0**, 1.0E6]
Width: waveguide width of the S-bend	[1.0, **1.1**, 1.0E6]
Wavelength [um]	[1.52,**1.55**,1.60]
simLoss: assumed propagation loss for circuit simulators [dB/cm]	[0.0, **0.5**, 1.0E6]

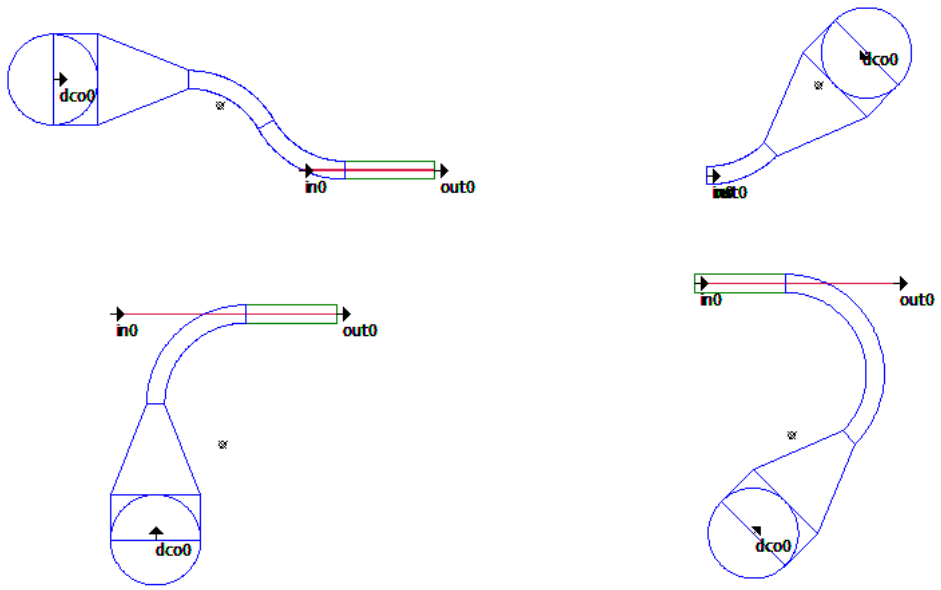
Optical ports: in0, out0	**DC ports:** None

BB folder: Electrics

BB name: LxDCpad	**Disclosure:** Public
Version: 1.0.0	**License:** Triplex Library
Replaces: None	**ReplacedBy:** None
Description: A probe pad with either a circular or a rectangular pad. Both types of pads have a fixed width of 100 µm, so that a lead of default width of 100 µm can directly be connected to it.	
 **dimension = 200, type = "Rectangle", length = 200**	
Parameters: dimension: pad diameter (circular) or width (rectangular) type: a circular pad or a rounded rectangle (corner radius 25 µm) length: pad height (only used for the rectangular type)	**Rangespec:** [100.0, **200.0**, 1.0E6] [Circle, **Rectangle**] [100.0, **200.0**, 1.0E6]
Optical ports: None	**DC ports:** dc0 = in0

BB folder: Electrics

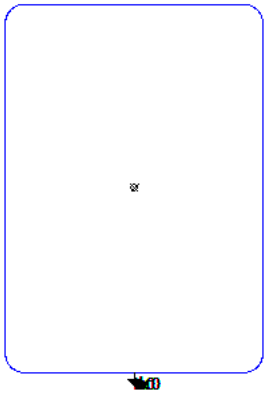
BB name: LxHeaterLead	**Disclosure:** Public
Version: 1.0.1	**License:** Triplex Library
Replaces: LxHeaterLeadHC v1.0.0	**ReplacedBy:** None
Description: To place a straight waveguide with a heater on top, and configuration of the lead shape and orientation.	



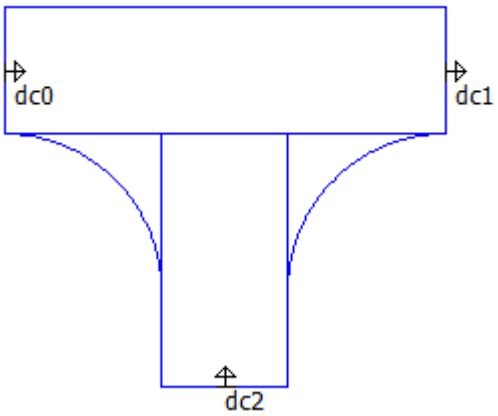
Parameters:	**Rangespec:**
location: specifies the direction of the pad w.r.t. the heater/waveguide	[**Left_Top**, Left_Bottom, Right_Top, Right_Bottom]
LeadAngle_deg: angle of the lead w.r.t. the waveguide	[0.0, **0.0**, 360.0]
heaterLength_um: heater length	[0.0, **100.0**, 1.0E6]
placeWaveGuide: Does a straight waveguide have to be placed?	[**True**, False]
radiusLead: : radius of curvature of the lead	[20.0, **100.0**, 1.0E6]

Optical ports: in0, out0	**DC ports:** dco0

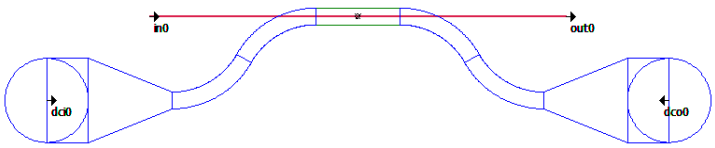
BB folder: Electrics

BB name: LxDCBondPad	**Disclosure:** Public
Version: 1.0.0	**License:** Triplex Library
Replaces: None	**ReplacedBy:** None
Description: A rectangular bondpad: for ground leads, the default size in the template is 350 µm × 500 µm. The other leads (the anodes) in the template the size is 350 µm × 300 µm.	
	
Parameters: dimension: pad diameter (circular) or width (rectangular) length: pad height (only used for the rectangular type)	**Rangespec:** [100.0, **350.0**, 1.0E6] [100.0, **500.0**, 1.0E6]
Optical ports: None	**DC ports:** dc0 = in0

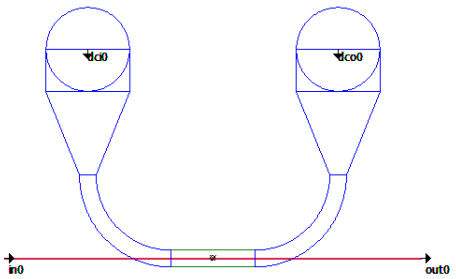
BB folder: Electrics

BB name: LxTjunctionLead	**Disclosure:** Public
Version: 1.0.0	**License:** Triplex Library
Replaces: None	**ReplacedBy:** None
Description: A rectangular bondpad: for ground leads, the default size in the template is 350 µm × 500 µm. The other leads (the anodes) in the template the size is 350 µm × 300 µm.	
	
Parameters: Length_Head: length of the head (part from DC port dc0 to dc1) Length_Body: length of the body (from DC port dc2 up to the head) Width: lead width of the Tjunction	**Rangespec:** [350.0, **350.0**, 1.0E6] [125.0, **200.0**, 1.0E6] [20.0, **100.0**, 1.0E6]
Optical ports: None	**DC ports:** dc0, dc1, dc2

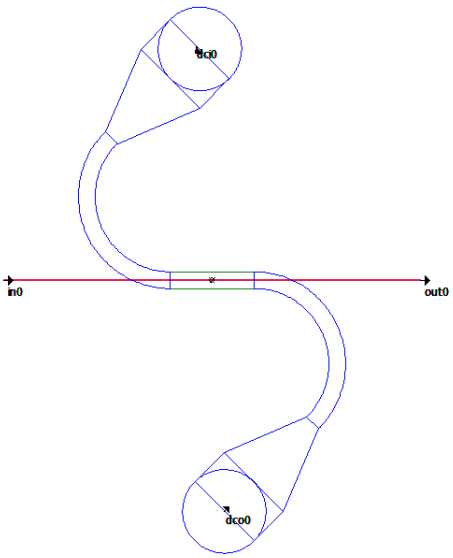
BB name: LxPhaseModulator	**Disclosure:** Public
Version: 1.0.2	**License:** Triplex Library
Replaces: LxPhaseModulator v1.0.1	**ReplacedBy:** None
Description: A straight optical waveguide with Thermo-Optical Phase Modulator based on a Cr heater with Cr/Au electrical leads. The orientation and shape of the input- and output leads can be controlled by specifying orientation (Lead1Up, Lead2Up) and the lead angles. The default value for the heater length is 2000 um which will produce the 2PI phase shift.	



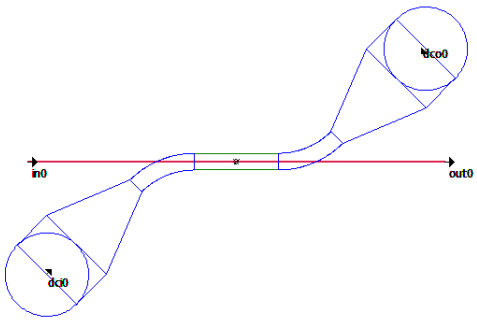
Lead1Up = Lead2Up = False, with both lead angles set to 0°.



Lead1Up = Lead2Up = True,
with both lead angles set to 90°.



Lead1Up = True, Lead2Up = False,
with both lead angles set to 135°.



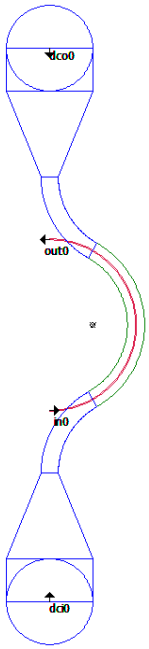
Lead1Up = False, Lead2Up = True,
with both lead angles set to 45°.

Parameters:	**Rangespec:**
HeaterLength: length straight heater	[0.1, **2000.0**, 1.0E6]
WaveguideLength: length straight waveguide	[0.1, **2100.0**, 1.0E6]
Width: width of the waveguide	[1.0, **1.1**, 1.0E6]
Lead1Angle: angle [°] of input/output lead #1 w.r.t. the waveguide	[-360.0, **0.0**, 360.0]
Lead2Angle: angle [°] of input/output lead #2 w.r.t. the waveguide	[-360.0, **0.0**, 360.0]
Lead1Up: Is lead #1 oriented upwards w.r.t. the waveguide?	[**True**, False]
Lead2Up: Is lead #1 oriented upwards w.r.t. the waveguide?	[**True**, False]
simDeltaTemp: heater temperature difference for circuit simulators [K]	[-1.0E6, **0.0**, 1.0E6]
simLoss: assumed propagation loss for circuit simulators [dB/cm]	[0.0, **0.5**, 1.0E6]

Optical ports: in0, out0	**DC ports:** dci0, dco0

BB name: LxPhaseModulatorArc	**Disclosure:** Public
Version: 1.0.2	**License:** Triplex Library
Replaces: LxPhaseModulatorArc v1.0.1	**ReplacedBy:** None

Description: A bent optical waveguide with Thermo-Optical Phase Modulator based on a Cr heater with Cr/Au electrical leads. The orientation and shape of the input- and output leads can be controlled by specifying orientation (Lead1Up, Lead2Up) and the lead angles. The option to apply the built-in straight-to-bend offsets (SBoffset) on the input and the output of the bent waveguides is available in this version. The built-in SBoffset is a function of wavelength, waveguide's width and bend radius, for TE polarization.



Lead1Up = Lead2Up = False, with both lead angles set to 60°.

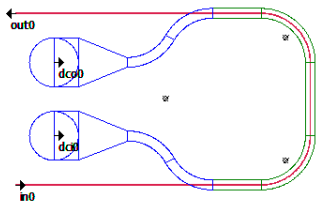
Parameters:	**Rangespec:**
HeaterAngle: angle bent heater [°]	[-360.0, **90.0**, 360.0]
WaveguideAngle: angle bent waveguide [°]	[-360.0, **80.0**, 360.0]
Width: width of the waveguide	[1.0, **1.1**, 1.0E6]
Radius: radius of curvature of the waveguide and the heater	[85.0, **100.0**, 1.0E6]
Lead1Angle: angle [°] of input/output lead #1 w.r.t. the waveguide	[-360.0, **0.0**, 360.0]
Lead2Angle: angle [°] of input/output lead #2 w.r.t. the waveguide	[-360.0, **0.0**, 360.0]
Lead1Up: Is lead #1 oriented upwards w.r.t. the waveguide?	[**True**, False]
Lead2Up: Is lead #1 oriented upwards w.r.t. the waveguide?	[**True**, False]
Wavelength [um]	[1.52,**1.55**,1.60]
simDeltaTemp: heater temperature difference for circuit simulators [K]	[-1.0E6, **0.0**, 1.0E6]
simLoss: assumed propagation loss for circuit simulators [dB/cm]	[0.0, **0.5**, 1.0E6]

Optical ports: in0, out0	**DC ports:** dci0, dco0

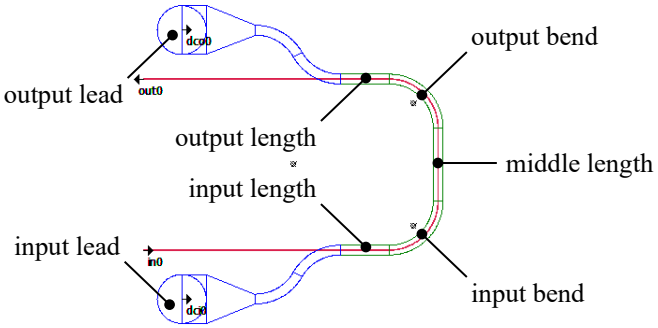
BB folder: Modulator

BB name: LxPhaseModulatorU	**Disclosure:** Public
Version: 1.0.1	**License:** Triplex Library
Replaces: LxPhaseModulatorU v1.0.0	**ReplacedBy:** None

Description: A U-shaped optical waveguide with Thermo-Optical Phase Modulator based on a Cr heater with Cr/Au electrical leads. The orientation and shape of the input- and output leads can be controlled by specifying orientation (Lead1Up, Lead2Up) and the lead angles. The option to apply the built-in straight-to-bend offsets (SBoffset) on the input and the output of the bent waveguides is available in this version. The built-in SBoffset is a function of wavelength, waveguide's width and bend radius, for TE polarization.



input_Lead = output_Lead = "inwards", with both lead angles set to 0°.

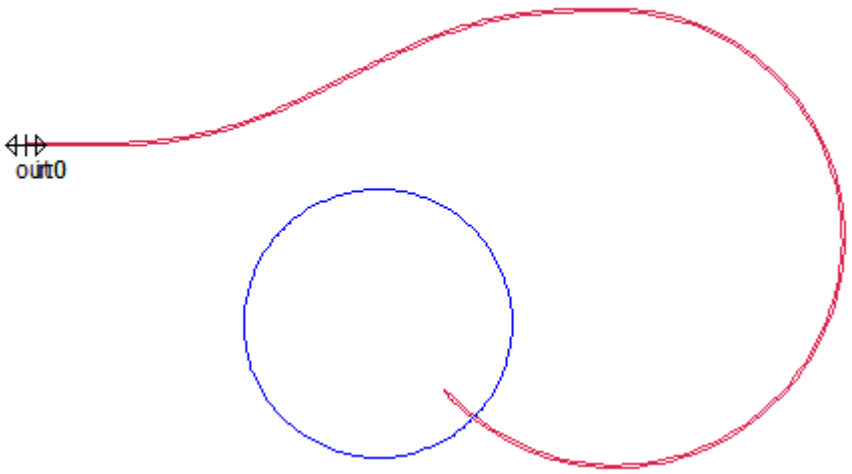


input_Lead = output_Lead = "outwards", with both lead angles set to 0°.

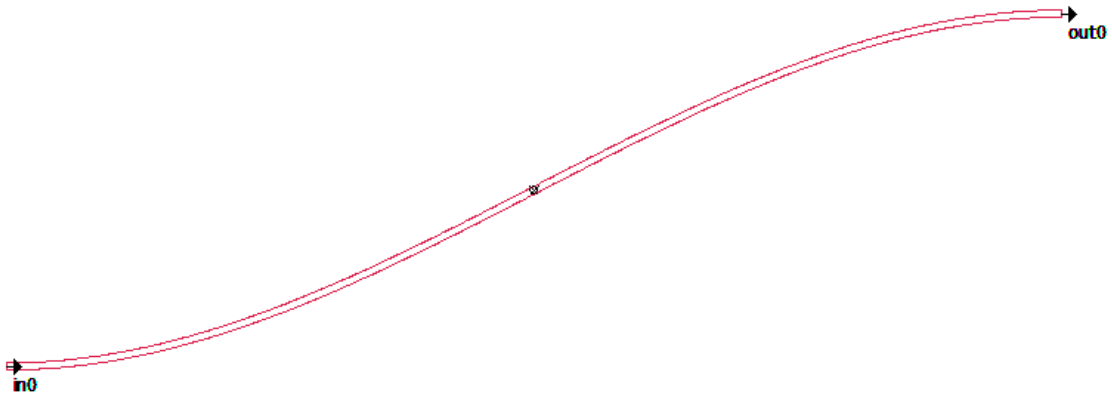
Parameters:	**Rangespec:**
input_BendRadius: radius of curvature of input heater/waveguide bend	[85.0, **100.0**, 1.0E6]
output_BendRadius: radius of curvature of output heater/waveguide bend	[85.0, **100.0**, 1.0E6]
input_BendAngle: angle [°] of input bend of heater/waveguide	[-360.0, **90.0**, 360.0]
output_BendAngle: angle [°] of output bend of heater/waveguide	[-360.0, **90.0**, 360.0]
input_WaveguideLength: length of input straight waveguide part	[0.1, **100.0**, 1.0E6]
output_WaveguideLength: length of output straight waveguide part	[0.1, **100.0**, 1.0E6]
middle_WaveguideLength: length of middle straight waveguide part	[0.1, **100.0**, 1.0E6]
input_HeaterLength: length of input straight heater part	[0.1, **100.0**, 1.0E6]
output_HeaterLength: length of output straight heater part	[0.1, **100.0**, 1.0E6]
input_Lead_Angle: angle [°] of input lead w.r.t. the waveguide	[-360.0, **0.0**, 360.0]
output_Lead_Angle: angle [°] of output lead w.r.t. the waveguide	[-360.0, **0.0**, 360.0]
input_Lead: orientation of input lead w.r.t. the waveguide	[**inwards**, outwards]
output_Lead: orientation of output lead w.r.t. the waveguide	[**inwards**, outwards]
WaveguideWidth: width of the waveguide	[1.0, **1.1**, 1.0E6]
Wavelength [um]	[1.52,**1.55**,1.60]

Optical ports: in0, out0	**DC ports:** dci0, dco0

BB folder: Termination

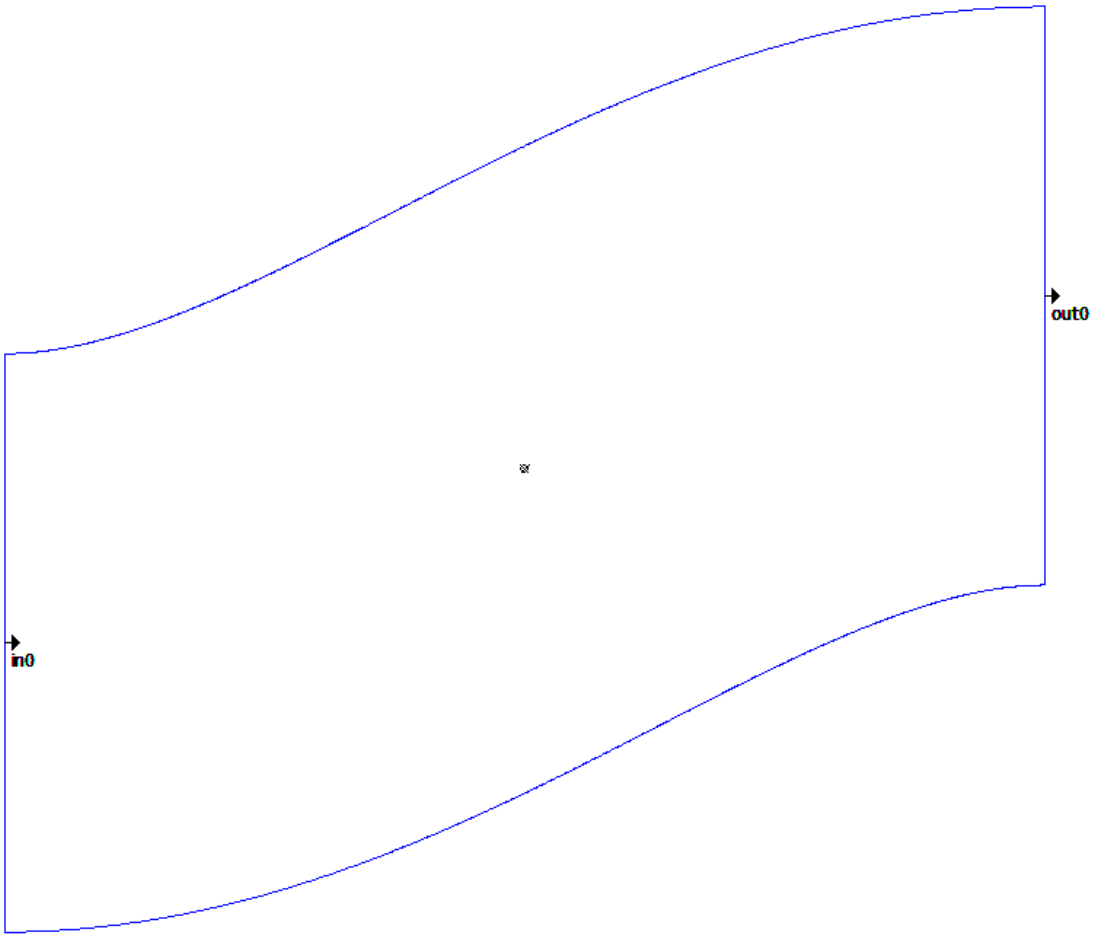
BB name: LxTermination	**Disclosure:** Public
Version: 1.0.0	**License:** Triplex Library
Replaces: None	**ReplacedBy:** None
Description: A tapered curve waveguide which ends with Cr/Au electrical lead. This building block is used to terminate the photonic circuit outputs which are not connected to the fiber array.	
	
Parameters: LengthStraight: length of the straight part of the beginning of the termination. LengthSine: length of the bend sine part of the termination. HeightSine: height of the bend sine part of the termination. arcRadius: radius of the bend polar at the end of the termination.	**Rangespec:** [0, **200.0**, 1.0E6] [0, **200.0**, 1.0E6] [-1.0E6, **50.0**, 1.0E6] [85.0, **100.0**, 1.0E6]
Optical ports: in0, out0	**DC ports:** None

BB folder: Connector

BB name: LxConnectorCurve	**Disclosure:** Public
Version: 1.0.1	**License:** Triplex Library
Replaces: LxConnectorCurve v1.0.0	**ReplacedBy:** None
Description: A Bezier curve between in0 and out0 (both ports have to be connected). The layout of the connector curve is based on a smooth curve and start and ends with a bent waveguide section with constant radius. This building block takes care of straight-to-bend offsets (SBoffset) on the input and the output of the connector. The built-in SBoffset is a function of wavelength, waveguide's width and curve radius at the input and the output of the connector, for TE polarization.	
	
Parameters: curveDerivative_input: derivative at the connector curve input curveDerivative_output: derivative at the connector curve output width1WG_um: waveguide width at connector curve input width2WG_um: waveguide width at the connector curve output Wavelength [um]	**Rangespec:** [-1.0E6, **1.0**, 1.0E6]\0.0 [-1.0E6, **1.0**, 1.0E6]\0.0 [1.0, **1.1**, 1.0E6] [1.0, **1.1**, 1.0E6] [1.52,**1.55**,1.60]
Optical ports: in0, out0	**DC ports:** None

BB folder: Connector

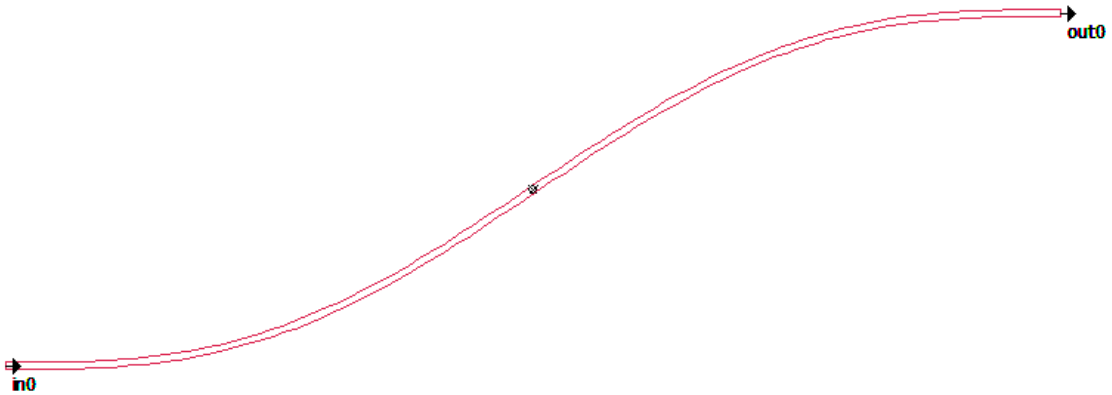
BB name: LxConnectorCurveDC	**Disclosure:** Public
Version: 1.0.1	**License:** Triplex Library
Replaces: LxConnectorCurveDC v1.0.0	**ReplacedBy:** None
Description: A Bezier curve between in0 and out0 (both ports have to be connected). The layout of the connector curve is based on a smooth curve and start and ends with a bent waveguide section with constant radius. This building block is intended to be used for leads and therefore straight-to-bend offsets are irrelevant.	



Parameters:	**Rangespec:**
curveDerivative_input: derivative at the connector curve input	[-1.0E6, **1.0**, 1.0E6]\0.0
curveDerivative_output: derivative at the connector curve output	[-1.0E6, **1.0**, 1.0E6]\0.0
width1WG_um: Lead width at connector curve input	[20.0, **100.0**, 1.0E6]
width2WG_um: Lead width at the connector curve output	[20.0, **100.0**, 1.0E6]

Optical ports: None	**DC ports:** in0, out0

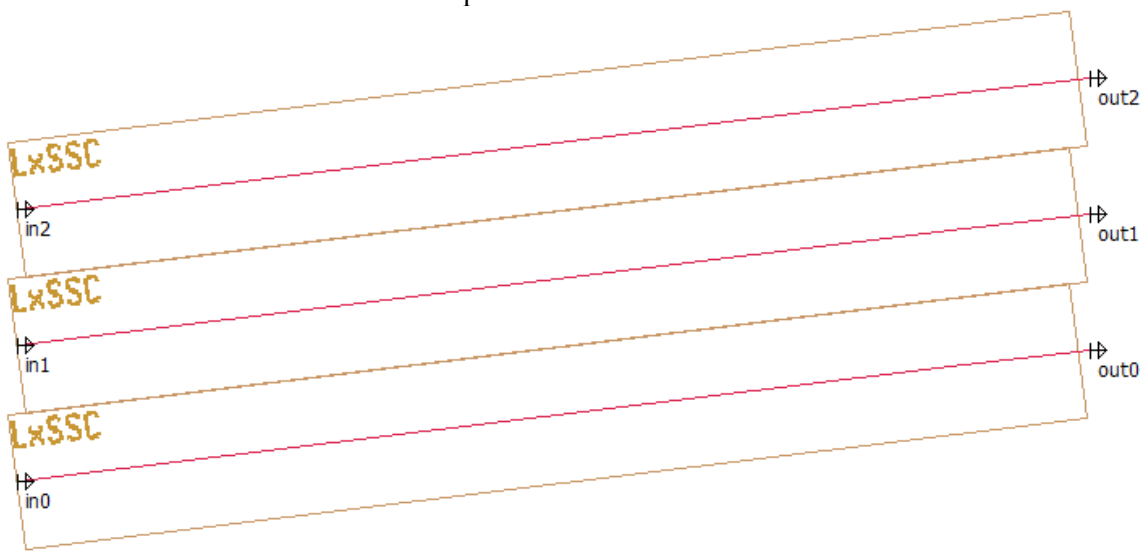
BB folder: Connector

BB name: LxConnectorSine	**Disclosure:** Public
Version: 1.0.1	**License:** Triplex Library
Replaces: LxConnectorSine v1.0.0	**ReplacedBy:** None
Description: A sine curve between in0 and out0 (both ports have to be connected). The layout of the connector curve is based on sinebend waveguides, so that straight-to-bend offsets do not have to be taken into account (as the connector has zero curvature at its input and output).	
	
Parameters: width1WG_um: waveguide width at connector curve input width2WG_um: waveguide width at the connector curve output	**Rangespec:** [1.0, **1.1**, 1.0E6] [1.0, **1.1**, 1.0E6]
Optical ports: in0, out0	**DC ports:** None

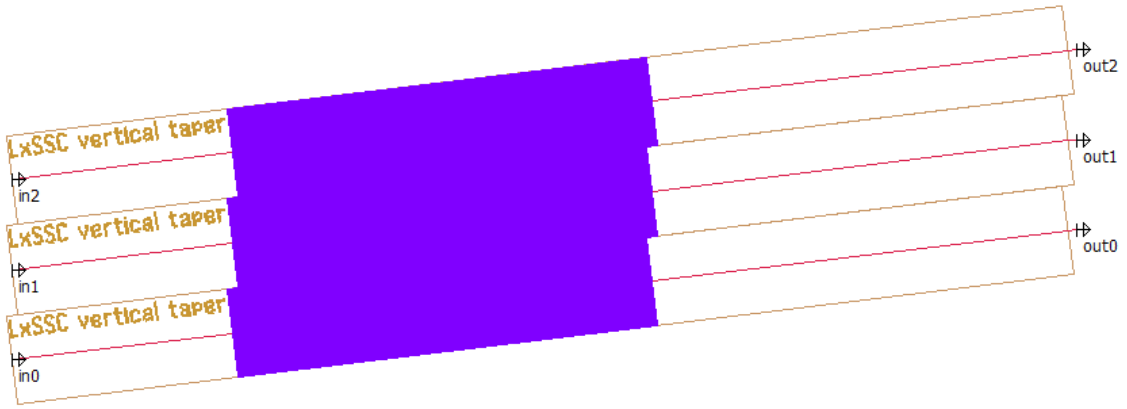
BB name: LxSSC	**Disclosure:** LioniX
Version: 1.0.1	**License:** Triplex Library
Replaces: LxSSC version 1.0.0	**ReplacedBy:** None

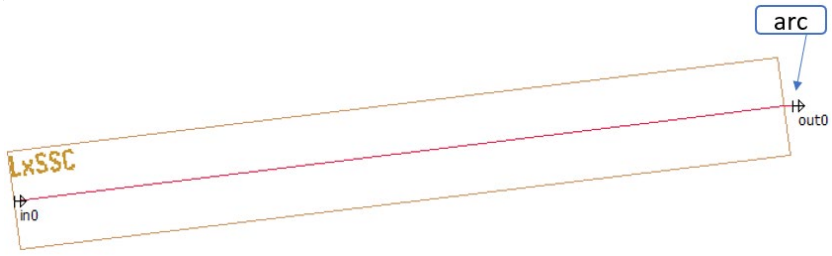
Description: A spot-size converter based on adiabatic vertical tapering of the guiding layers, in combination with a lateral tapering. If the SSC array is placed under a non-zero angle, a bent waveguide would be added at the end to go back to a zero angle by default. The bend is based on LxArc and therefore also takes care of straight-to-bend offsets (SBoffset). The value of the SBoffset in this private building block is defined for wavelength 1.55 um, TE polarization, bend radius 100 um, and waveguide width within range 1.0 um until 3.0 um. It is important that waveguides are not placed too close to the place where the vertical tapering will take place, therefore the DRC will not allow waveguide structures closer than 600 µm in vertical direction.

Below is the LxSSC without vertical taper:



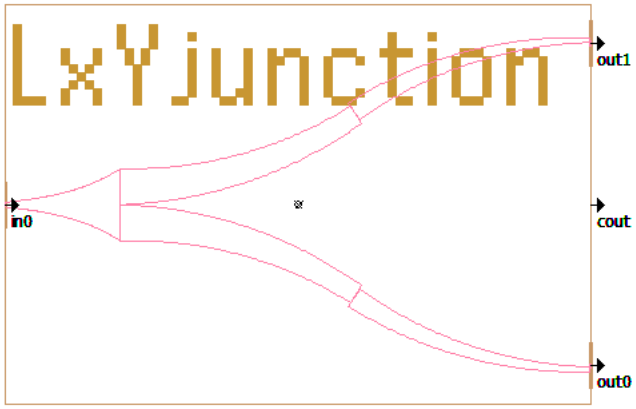
Below is the LxSSC with vertical taper to get the best mode coupling from the LxADS high index contrast platform to the low index contrast platform such as standard glass fiber (MFD 10 um):



Parameters:	**Rangespec:**
angle: angle of the SSC array at the chip end-facet [°] To find the tilted angle for the SSC, we can use the Snel law: nLx*sin(angle)=n_otherPlatform*sin(angle_otherPlatform). nLx and n_otherPlatform are the effective index of Mode0 TE at the end-facet. If the end facet is LioniX ADS low index contrast, then nLx = 1.4462. If the end facet is LioniX ADS high index contrast, nLx = 1.530 ± 0.005. If we would like to connect our LioniX ADS chip to the InP chip: if the SSC in the InP chip has the tilted angle 7° to 9°, then the SSC in the LioniX ADS chip has tilted angle ~ 18° to 21°.	[-180.0, **0.0**, 180.0]
number_of_fiber: number of SSCs (N) in the array.	[>0,**1**]
pitch: vertical pitch between the waveguides of the SSC at the chip end-facet.	[127.0, **127.0**, 1.0E6]
wgWidth_endFacet: width of the waveguide at the end-facet **wgWidth_onChip:** width of the waveguide at the on-chip side	[0.8, **0.8**, 3.0] [1.0, **1.1**, 3.0]
PlaceVerticalTaper Since MPW 16, there is an option to use the vertical taper in the LxSSC to get a better coupling from the LxADS high index contrast platform to the low index contrast platform such as glass fiber. To use vertical taper, set the checkmark on the parameter PlaceVerticalTaper You can choose <u>not</u> to use the vertical taper if you would like to couple your LxADS chip to another high index contrast platform such as to some indium phosphide (InP) foundries. Vertical Taper is <u>not</u> needed if the mode field from LxADS high index contrast platform matches the mode field from the other platform you would like to connect to.	[0,**1**] This is a Checkmark sign: 0=no, 1=yes.
addArc_atOutput: If the SSC angle is not zero, you can add the arc at the output of the SSC at the on-chip side. This arc enables you to connect your chip layout to the tilted SSC. You can disable the arc by setting this parameter to zero. 	[0,**1**] This is a Checkmark sign: 0=no, 1=yes.

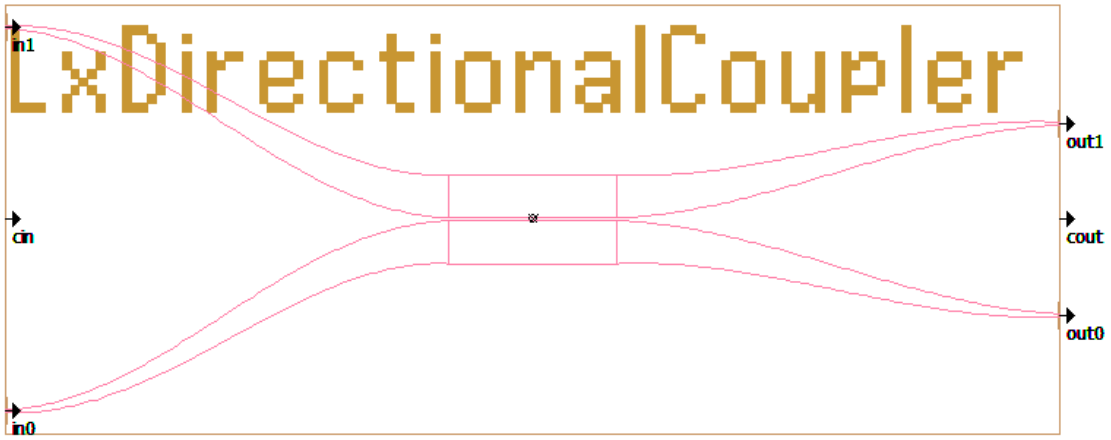
Optical ports: in0, ...,in(N-1); out0,...,out(N-1)	**DC ports:** None

BB folder: Splitter

BB name: LxYjunction	**Disclosure:** LioniX
Version: 1.0.1	**License:** Triplex Library
Replaces: LxYjuncHC v1.0.0	**ReplacedBy:** None
Description: A wavelength independent, polarisation independent optical 50%/50% (±10%) power splitter based on a Y-junction with blunt. This component will have an additional loss of 0.5 dB. N.B.: The real mask data will not be shared. To give the designer a guide to the eye, instead of the real mask data, a mockup is shown in a different mask layer (mcsWAVEGUIDE_nogds), using unrealistic parameters.	
	
Parameters: Pitch: pitch of the output waveguides simLoss: assumed propagation loss for circuit simulators [dB/cm]	**Rangespec:** [20.0, **127.0**, 1.0E6] [0.0, **0.5**, 1.0E6]
Optical ports: in0, out0, out1, cout	**DC ports:** None

BB folder: Coupler

BB name: LxDirectionalCoupler	**Disclosure:** LioniX
Version: 1.0.1	**License:** Triplex Library
Replaces: LxDirCouplerHC v1.0.0	**ReplacedBy:** None
Description: An optical 50%/50% (±10%) power splitter for TE polarised light at 1550 nm wavelength based on a directional coupler. This component will have an additional loss of 0.5 dB. N.B.: The real mask data will not be shared. To give the designer a guide to the eye, instead of the real mask data, a mockup is shown in a different mask layer (mcsWAVEGUIDE_nogds), using unrealistic parameters.	



Parameters:	**Rangespec:**
PitchIn: pitch input waveguides	[100.0, **127.0**, 1.0E6]
PitchOut: pitch output waveguides	[100.0, **127.0**, 1.0E6]
simLoss: assumed propagation loss for circuit simulators [dB/cm]	[0.0, **0.5**, 1.0E6]

Optical ports: in0, in1, out0, out1, cin, cout	**DC ports:** None

9 Mask file generation

When you have finished your design, in the PhoeniX software one can generate the mask files by pressing the "Start" button: then the design rule check will be carried out, and in totally 9 different files will be generated (of type .gds, .map, .spt, .txt, .html). Please send all these files to LioniX International.

10 Schedule

Participants to this run are invited to follow a workshop and training to get acquainted with TriPleX™ technology, Building Block library and the mask design software (OptoDesigner) which will be used to define the maskfiles.

Important dates:

Designs ready	September 2018
Fabrication process finished	January 2019

11 Contact

For more information, and for design submission, please send an e-mail to **MPW@lionix-int.com**. The participants are encouraged to discuss their designs in an early stage with LioniX International engineers to get feedback and to determine required footprint.

12 References

[1] F. Morichetti, et al (2007) "Box-Shaped Dielectric Waveguides: A New Concept in Integrated Optics?", Journal of Lightwave Technology, 28 (7). pp. 2579-2589. ISSN 0733-8724.

[2] STW research program (Netherlands): "Generic Technologies for Integrated Photonics (GTIP)", June 2010.

[3] U.S. Patent nr. 7,146,087, "Low nodal birefringent waveguides and method of fabrication", May 2006.

[4] R.G. Heideman et al, "Large-scale integrated optics using TriPleX™ waveguide technology: from UV to IR", SPIE Photonics West, 24-29 Jan 2009, San Jose, California, U.S.A.

[5] J. F. Bauters, et al. "Ultra-low loss silica-based waveguides with millimeter bend radius," ECOC (Torino, Italy, 2010).

[6] A. Meijerink et al.(2010) "Novel ring resonator-based integrated photonic beamformer for broadband phased array receive antennas - part I: design and performance analysis", Journal of Lightwave Technology, 28 (1). pp. 3-18. ISSN 0733-8724.

[7] L. Zhuang, et al. (2010) "Novel ring resonator-based integrated photonic beamformer for broadband phased array receive antennas - part II: experimental prototype". Journal of Lightwave Technology, 28 (1). pp. 19-31. ISSN 0733-8724.

[8] A. Leinse, et al., "The life marker chip for the Exomars mission", Invited presentation at IP2011 (Ottawa, Canada, 2011).

[9] Heideman, R.G. and Geuzebroek, D.H. and Leinse, A. and Melloni, A. and Morichetti, F. and Roeloffzen, C.G.H. and Meijerink, A. and Zhuang, L. and van Etten, W.C. and Klein, E.J. and Driessen, A. (2007) *Low loss, high contrast optical waveguides based on CMOS compatible LPCVD processing.* In: Proceedings European Conference on Integrated Optics (ECIO), 27-28 April 2007, Copenhagen, Denmark.

[10] K. Wörhoff, R.G. Heideman, A. Leinse, M. Hoekman, *TriPleX: A Versatile Dielectric Photonic Platform – Review Article (Open Access)*, Adv. Opt. Techn. 4(2), 2015, pp. 189–207.

APPENDIX 1 Design rules for Characterization Packaging for IR (Version 1.2)

1 Introduction

LioniX International has developed a standard packaging service called Characterization Packaging Standard (CPS). The philosophy behind this is to facilitate characterization and provide optimal coupling from chip to fiber. Chip sizes produced in MPW runs are suitable for this standard packaging, provided the CPS design rules are met.

The focus of the service is to provide customers with an off-the-shelf solution for the packaging and actuation (e.g. of phase-shifters) of their PIC. This allows the customer to focus fully on the characterization of the functionality of the PIC without the need to spend time and resources on technical and logistical details such as the design, fabrication, assembly and programming of the chip package with fiber-pigtails and control electronics.

To achieve a standard packaging service the various packaging options have been standardized and are therefore bound to certain design rules. In Chapter 2 an overview of the standard types of assemblies are given. In Chapter 3 the design rules that need to be followed in order to be eligible for packaging are stated. Chapter 4 will show some common mistakes.

2 Assembly types

In Figure 16 an impression of the CPS assembly is given. The assembly consists of the following parts

- A gold-plated copper base, called a submount.
- Strain relief for the fiber array(s).
- Interface PCBs with Flat Flex Connectors (FFC).
- (optional) a laser current connector (2 pins).
- The optical subassembly pigtailed with fiber-arrays and/or laser section.
- A protective cover to protect the wire bonds

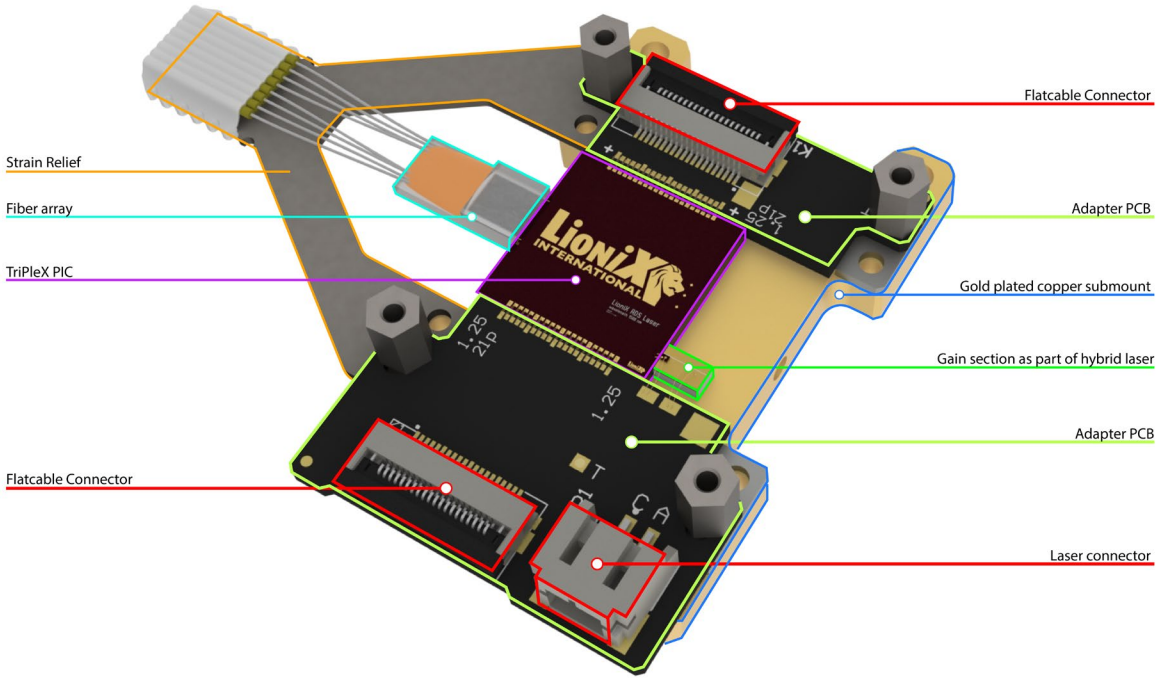


Figure 16: Example of a CPS laser assembly, protective cover for the assembly not shown in the figure.

In the CPS standard 4 types of assemblies are offered (a graphical overview is shown in Table 2):

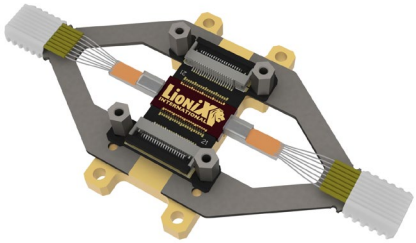
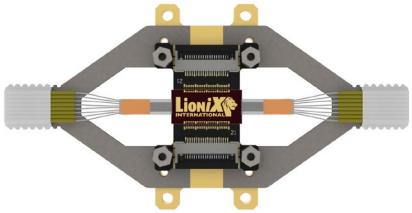
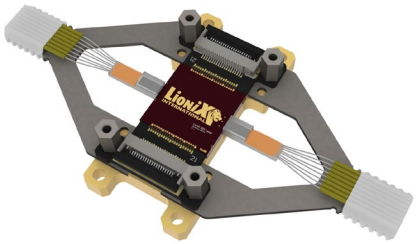
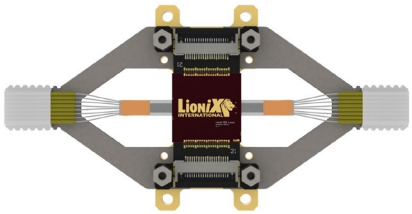
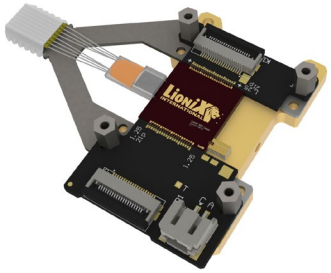
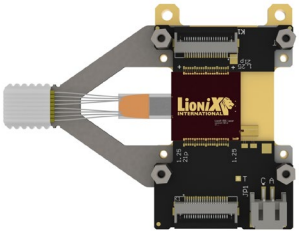
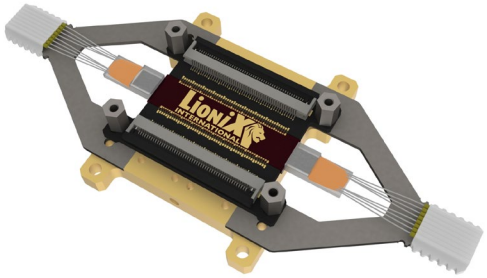
1. 16 mm wide x 8 mm high on a copper submount.
2. 16 mm wide x 16 mm high on a copper submount.
3. 16mm wide x 16 mm high with integrated laser on a copper submount.
4. 32 mm wide x 8 mm high on a copper submount.

The connector types and order codes for element 14 are stated in Table 1.

Table 1: Components used on adapter PCBs

Connector Type	Used in (assembly #)	Part number (element14)
20 Pins 0.5mm FFC	#1#2#3	2470705
50 Pins 0.5mm FFC	#4	2470718
2 Pins laser connector	#3	9492615
20 position ribbon cable	#1#2#3	1908528
50 position ribbon cable	#4	1908564

Table 2: Overview of different types of assemblies

#1	16 x 8 mm device on a copper submount.
	
#2	16 x 16 mm device on a copper submount.
	
#3	16 x 16 mm device with laser on a copper sub-mount.
	
#4	32 x 8 mm device on a copper submount.
	

3 Design rules for packaging

The design rules that need to be considered before a design can be packages are summarized in the following list. The flowchart Figure 17 given in will help understand the design rules.

- Dimension Chip size
- Fiber array position
- Alignment features required for pigtailing.
- Bond pads (location and size)

Some important notes to consider when you are doing packaging:

1) *Only the following sizes are eligible for packaging:*
   a. *16x8 mm*
   b. *16x16 mm*
   c. *16x16 mm with laser*
   d. *32x8 mm*

2) *The device can only be pigtailed if the standard Spot Size converters are used. Moreover, the array needs alignment loops discussed in xx.*

3) *If you require wire bonding, you will require one of the standard bond pad layouts stated in x. Other layouts can be fabricated* ***but will NOT be bonded.***

4) *In the case of a hybrid laser assembly, this can only be done by using the 16x16mm with laser schematic. This also requires and extra alignment port on the fiber array.*

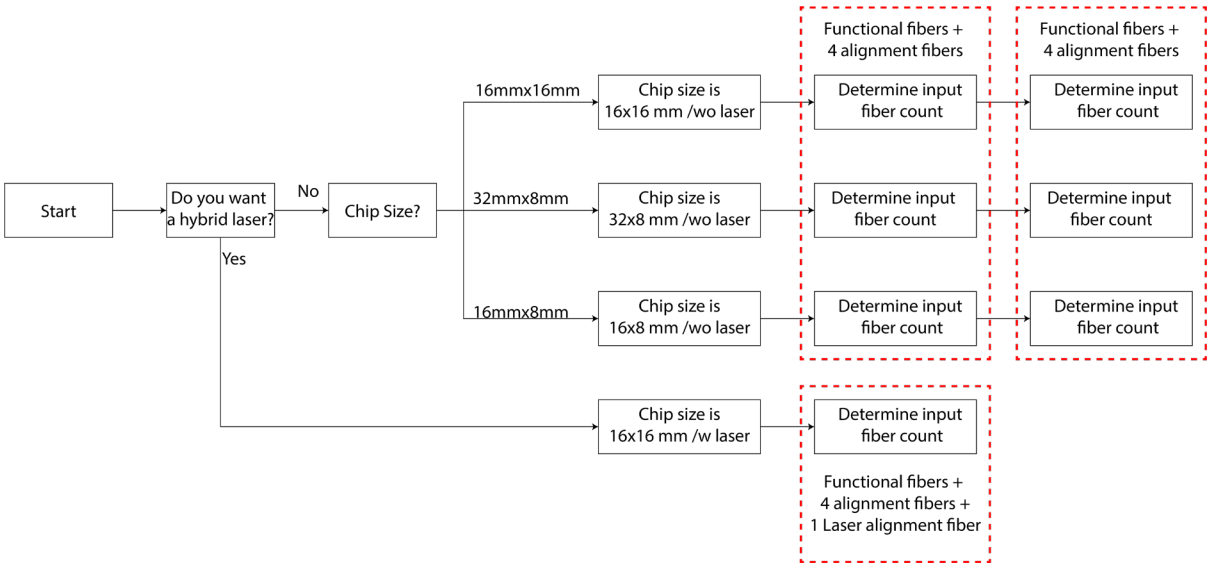


Figure 17: Flowchart for determining which assembly type to order.

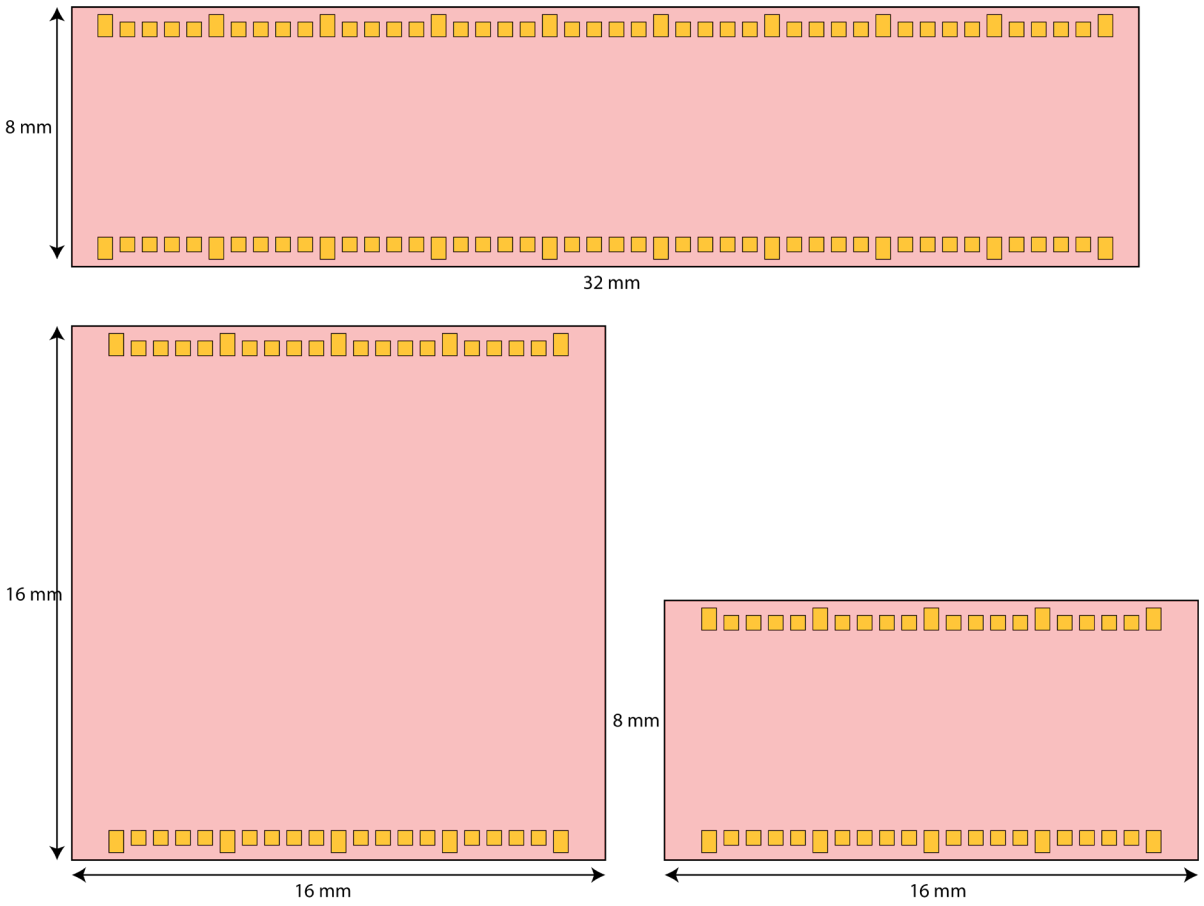
3.1 Chip size and definition of dimensions

The CPS supports packaging of PICs having the following sizes:

Table 2.1: Supported chip sizes.

Chip size type #	Length (mm)	Width (mm)
#1	16	16
#2	32	8
#3 (incl. Laser)	16	16
#4	16	8

The chip sizes including bondpad layouts are given in the figure below:



3.2 Selection of the fiber array(s)

The CPS supports the fiber-pigtailing with fiber arrays having 8, 16 or 32 channels, on one or both sides. The PICs can be pigtailed using a standard SMF fiber array or a PM fiber array connectorized with FC-APC connectors. The length of the fibers in the array is 1m.

The connectors and the fibers in the PM fiber array have the polarization axis oriented as indicated in Figure 18 an Figure 19.

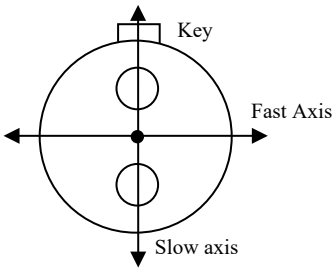


Figure 18: ***Figure 2.4a. Polarization axis in FC-PC connector.***

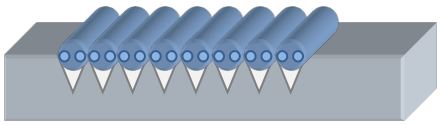


Figure 19: Orientation of fibers in the fiber array used with NIR PICs.

Note that the number of channels in the fiber array should always be at least 4 more than the number of channels required to address the on-chip functionality. This is because the outermost two fibers on each side in the fiber array are always reserved as **alignment waveguides**. These waveguides are required for the active optical alignment procedure used to align and attach a fiber array to the PIC. For the chip to be eligible for packaging the user should use the configuration shown in Figure 20.

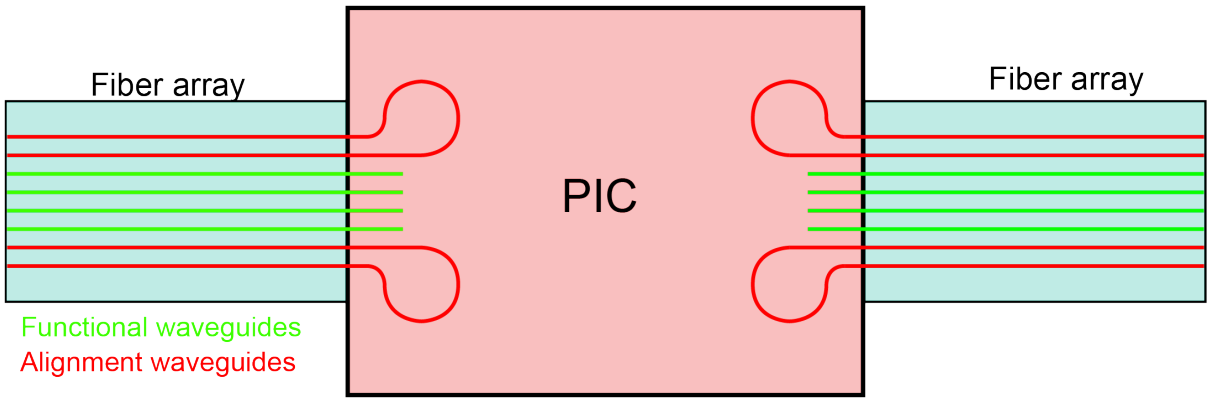
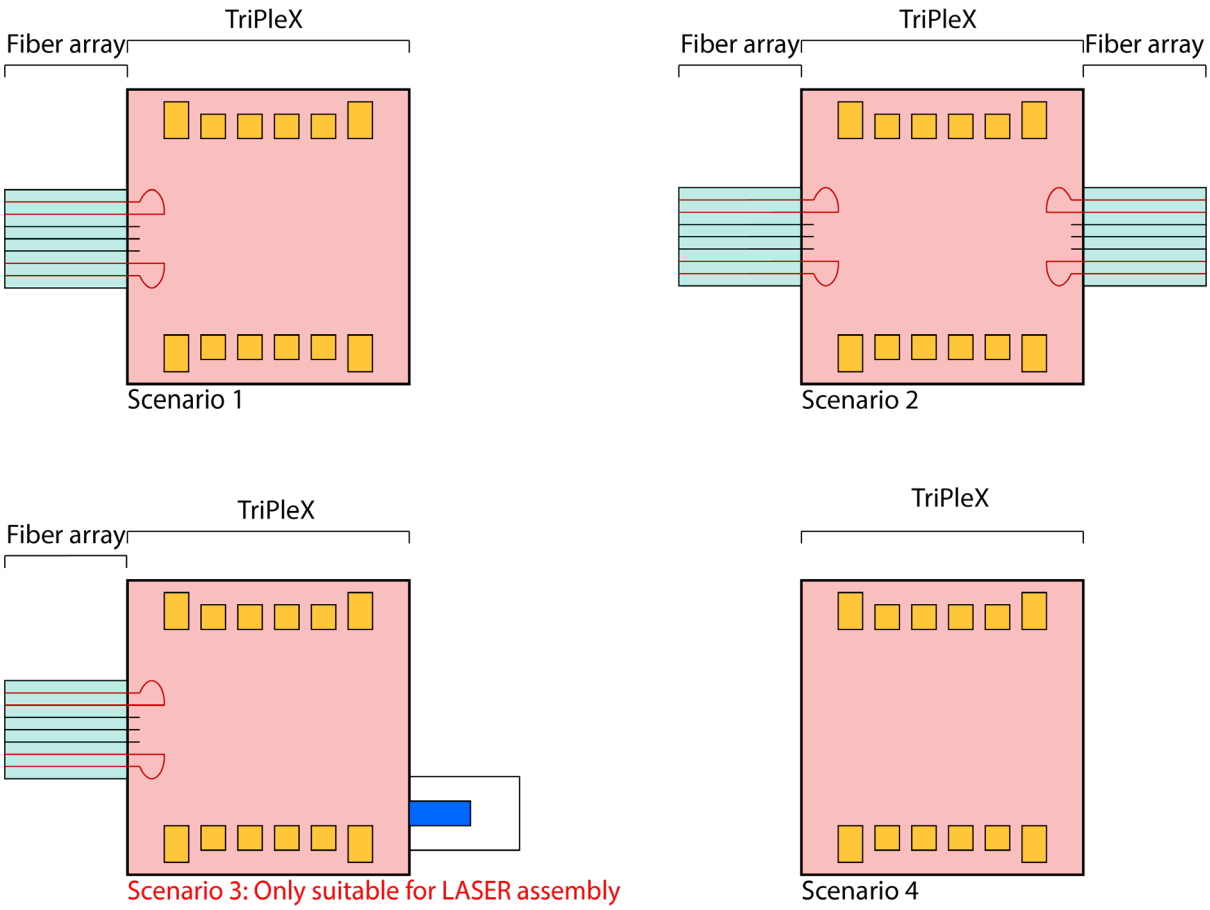


Figure 20: Configuration required for assembly.

The bond pads should be oriented along the length of the chip. The fiber arrays should be oriented along the perpendicular facets. The following scenarios are possible.

Important Please be aware that a very common mistake is that an assembly is ordered only counting the functional fibers. This is not the appropriate way! If, for example, 4 functional fibers are needed, an 8-channel fiber array should be ordered! Moreover, the fibers array should be located in the center and there are no open slots allowed!



Note: **The fiber array should be placed on the center of the facet.**

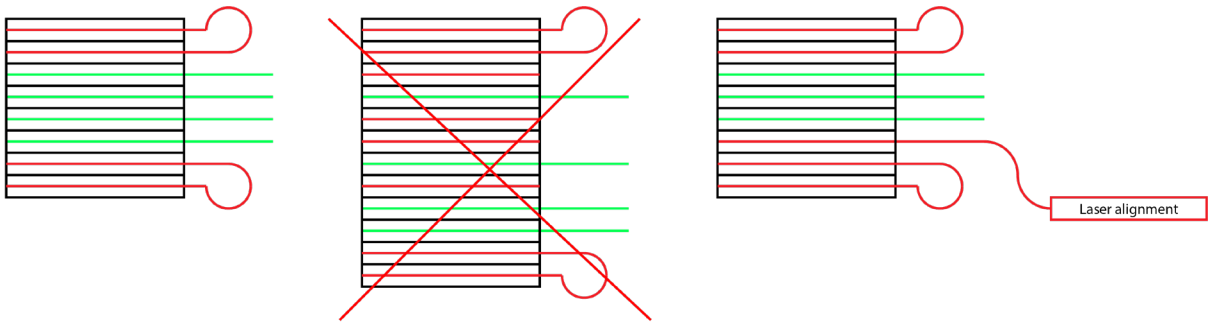


Figure 21: Fiber array count for assemblies. A) 4 functional fibers with 4 alignment fibers. Order 8 channel fiber array. B) 4 functional fibers with 4 alignment fibers, but with open spaces, do not do this as in this case a 16 channel fiber array is required for 8 fibers. C) 3 functional fibers 5 alignment fibers. In case of a hybrid laser assembly, an extra alignment fiber is needed for the laser.

3.3 Submount

After the photonic sub-assembly is completed the sub-assembly is fixed to a copper submount. The submount improves handling, acts as a heat sink for the PIC and provides support and strain relief for the fiber arrays. Finally, it acts as a base to mount PCBs to form a stable base for wire bonding. The CPS provides three standard submount types.

PICs that have a length of 16 mm, and do not have a hybrid laser, will be placed on submount type sA. The mechanical drawing for submount type sA is shown in Figure 22 and Figure 23.

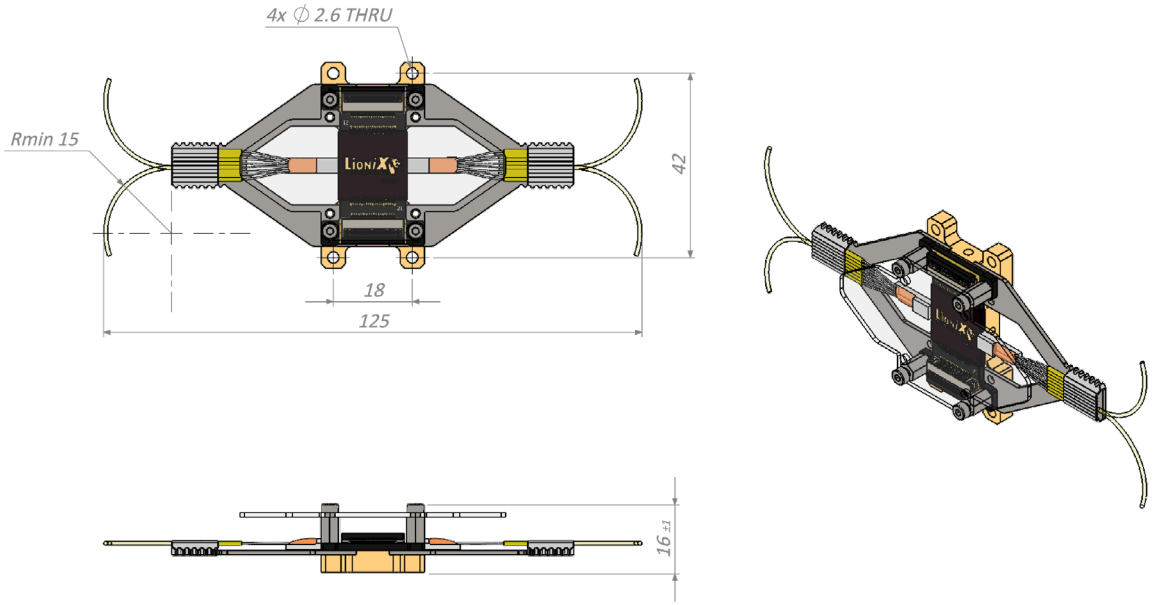


Figure 22: Overview of the dimensions for submount type sA (plastic cover not drawn in the picture).

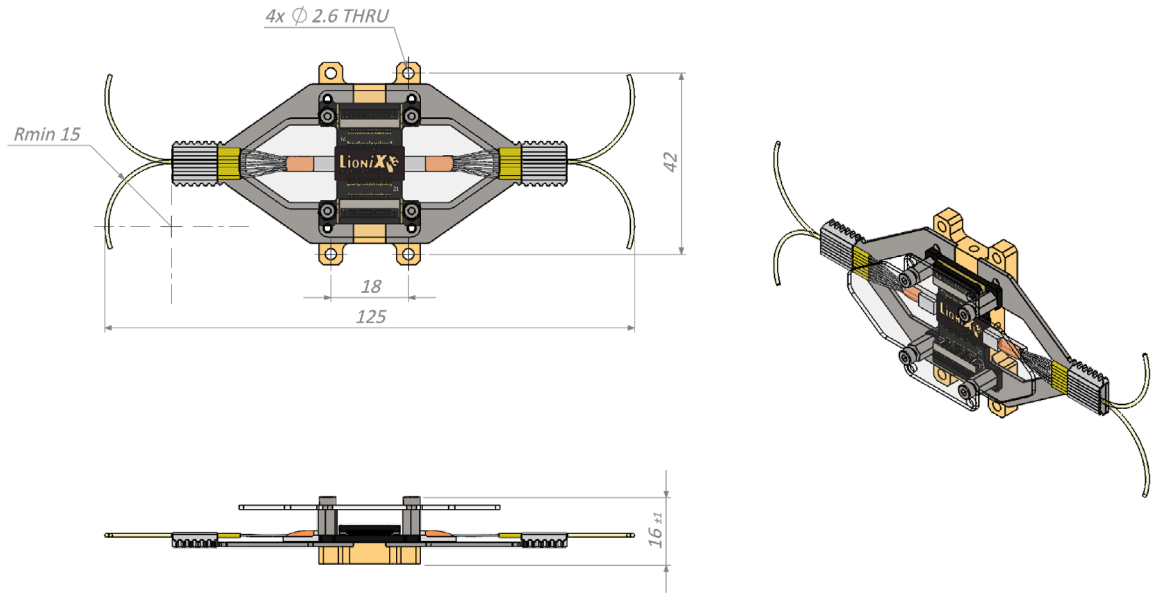


Figure 23: Overview of the dimensions for submount type sA with a 16x8 mm chip (plastic cover not drawn in the picture).

PICs that have a length of 16 mm, and are assembled together with a hybrid laser, will be placed on submount type sB. The mechanical drawing of submount type sB is shown in Figure 24.

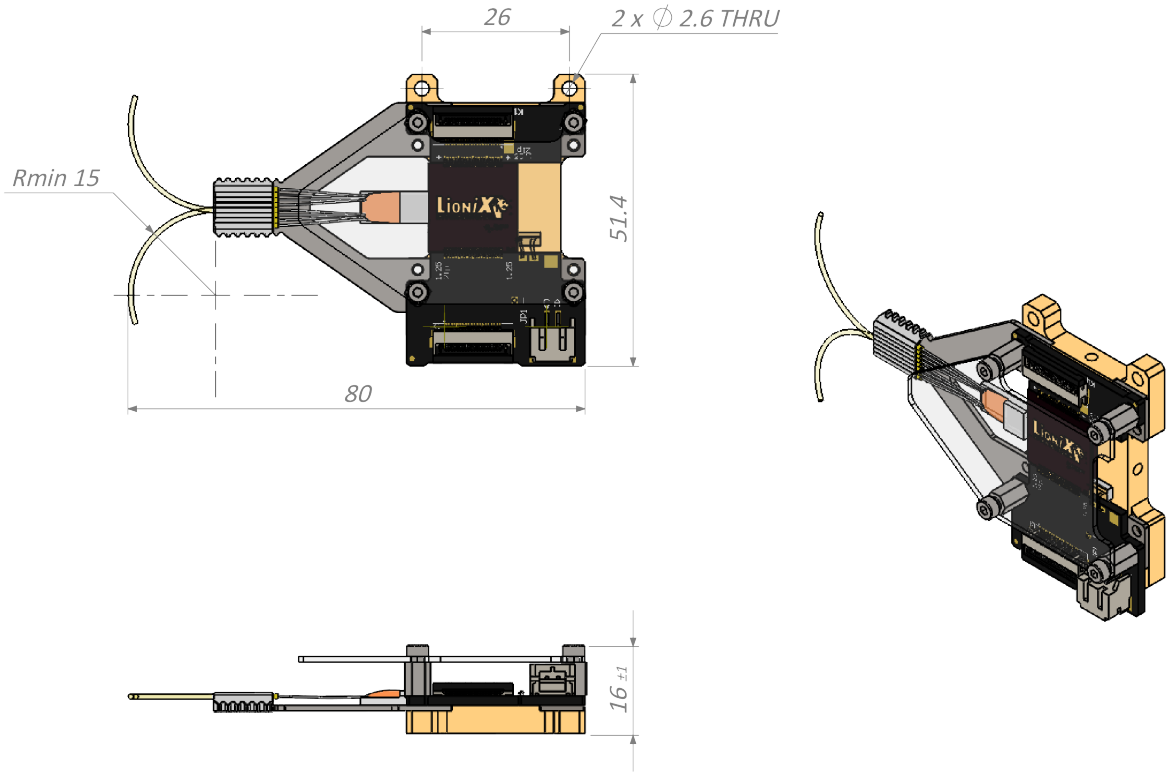


Figure 24: Overview of the dimensions for submount type sB (plastic cover not drawn in the picture).

PICs that have a length of 32 mm will be placed on submount type sC for which the mechanical drawing and rendering are given in Figure 25.

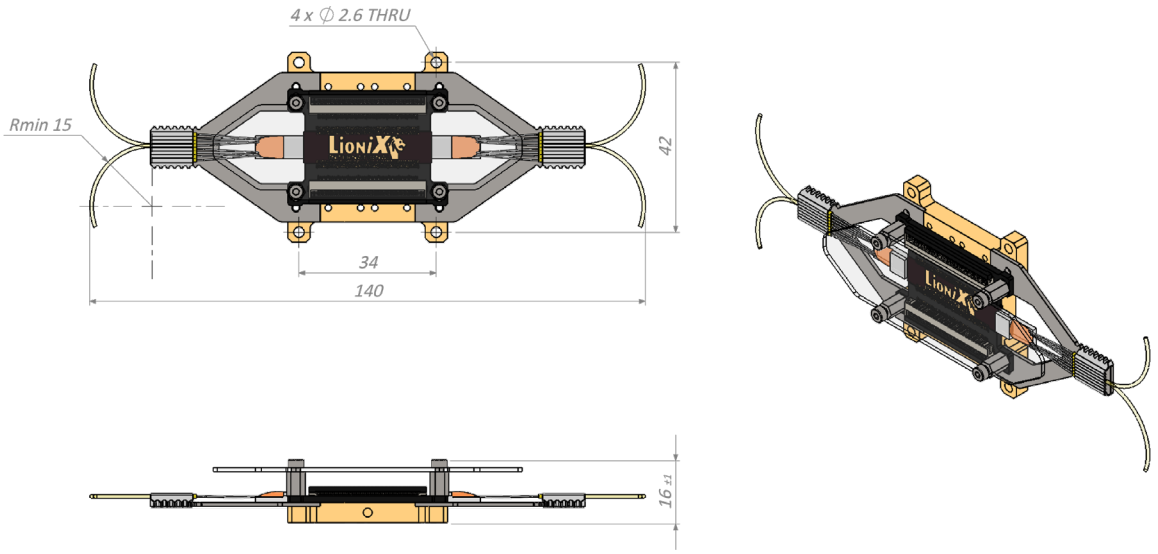


Figure 25: Overview of the dimensions for submount type sC (plastic cover not drawn in the picture).

Table 2.2: Supported chip dimensions

Chip size type #	Length (mm)	Width (mm)	Will use CPS submount type:
#1	16	8	sA
#2	16	16	sA
#3	16	16	sB
#4	32	8	sC

3.4 Wirebonding of the PIC

The wire-bonding of a PIC greatly simplifies the access to on-chip electrical (e.g. heater actuator) functionality. The wirebonds are made using gold wedge-wedge bonding to one or two "wire-bond to FCC connector adapter PCBs" which are fixed at the top and/or bottom edge of the PIC. The adapter PCBs come in 3 different types configurations. The adapter PCBs and the PIC design rules for both categories are discussed in the following sections. **Anything deviating from these standard configurations will not be wire bonded.**

3.4.1 Wirebond adapters for chip width of 16 mm, without laser.

For the 16 mm wide designs, where the number of actuators is lower than 16 on each side, standard PCBs are mounted and wire bonded to the PIC. The Bond pads will fanout to a flatcable connector to facilitate the access to the actuators. In Figure 26, the configuration of the PCB and the connections of the 16mm wide wirebond adapter are shown.

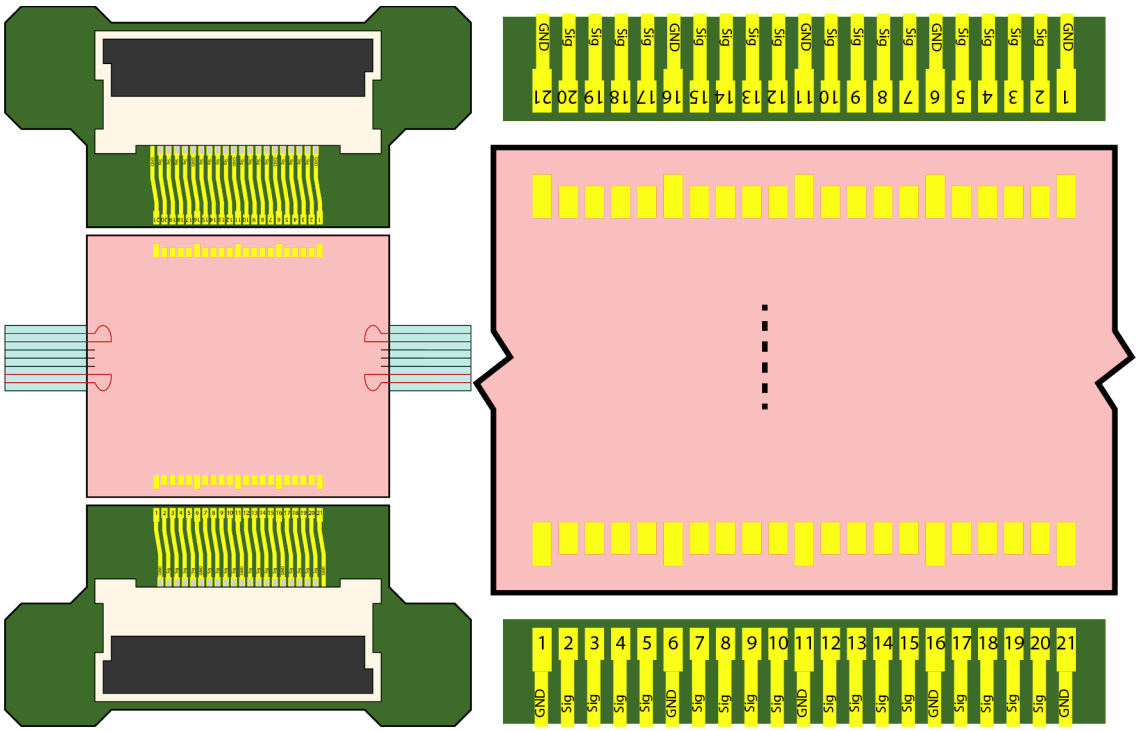


Figure 26: Bondpad configuration of a 16x16 mm chip without laser.

3.4.2 Wirebond adapters for chip width of 16 mm, with laser.

For the 16x16mm designs where the number of actuators is lower than 16 on each side and there is a hybrid laser assembly, standard PCBs are mounted and wire bonded to the PIC. The Bond pads will fanout to a flatcable connector to facilitate the access to the actuators. Moreover the PCB will provide an interface to the laser section. In Figure 27, the configuration of the PCB and the connections of the 16mm wide wirebond adapter with laser are shown.

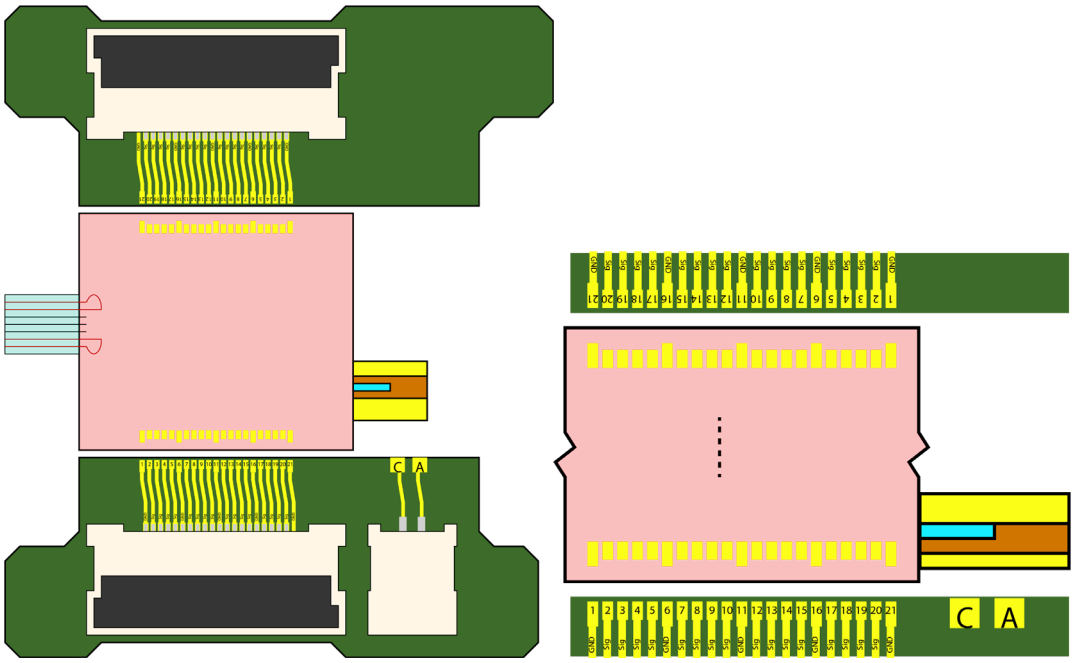


Figure 27: Bondpad configuration of a 16x16 mm chip with hybrid laser.

3.4.3 Wirebond adapters for chip width of 32 mm, without laser.

For the 32x8mm designs where the number of actuators is lower than 40 on each side, standard PCBs are mounted and wire bonded to the PIC. The Bond pads will fanout to a flatcable connector to facilitate the access to the actuators. In Figure 28 the configuration of the PCB and the connections of the 32 mm wide wirebond adapter without laser are shown.

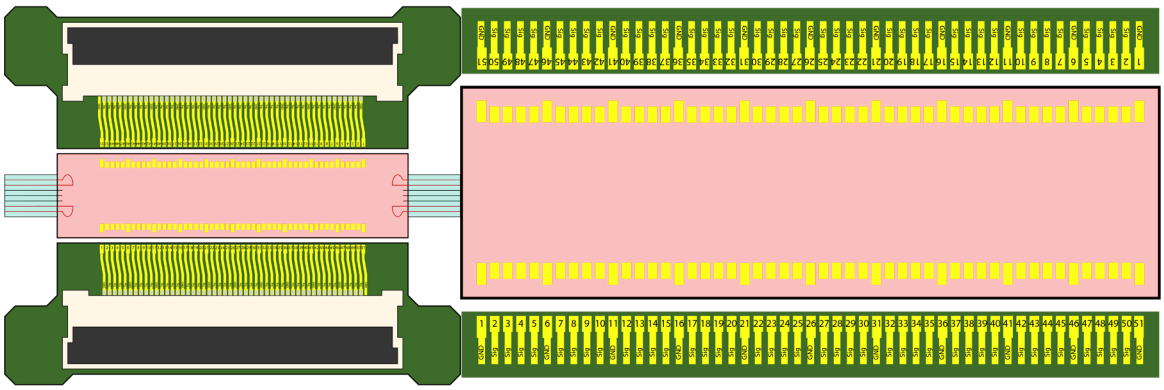


Figure 28: Bondpad adapter for PICs with a length of 16 and a maximum of 32 actuators

3.4.4 Bond pad specification

Regular bondpads that connect to drive leads measure 350x300 µm. Ground bondpads measure 350x500 µm. The first and then every fifth bondpad is required to be a ground bondpad. The distance between bondpads is 150 µm, making the bondpad pitch 500 µm. Bondpads should be placed at 300 µm from the edge of the PIC. The bondpad definition is shown in **Error! Reference source not found.**.

The position of the first bondpad with respect to the input facet, d, is specific to the combination of bondpad adapter type and the length of the PIC. For bondpads placed at the bottom edge of the PIC, d is measured from the left facet. For bondpads placed at the top edge of the PIC, d is measured from the right facet.

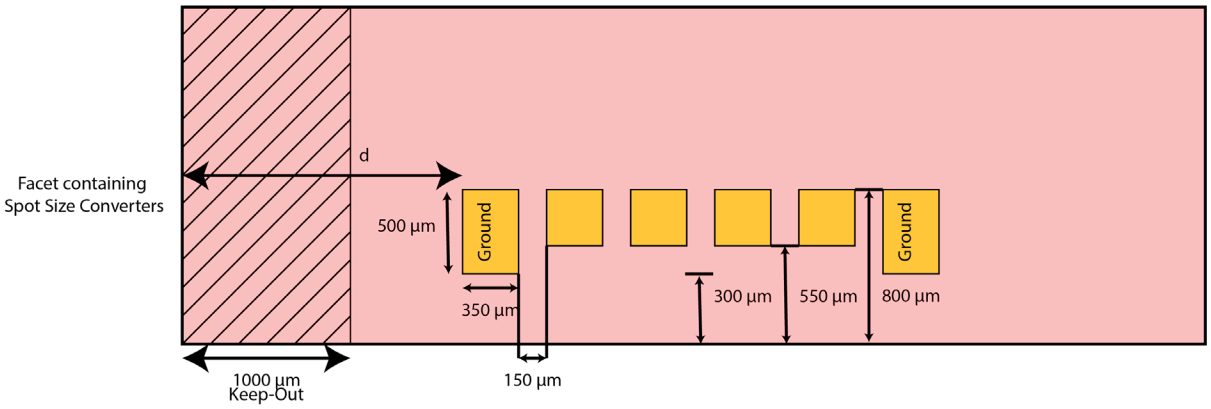


Figure 29: Bondpad definition required for assembly.

The distance ***d*** for different assembly types is given in Table 7.

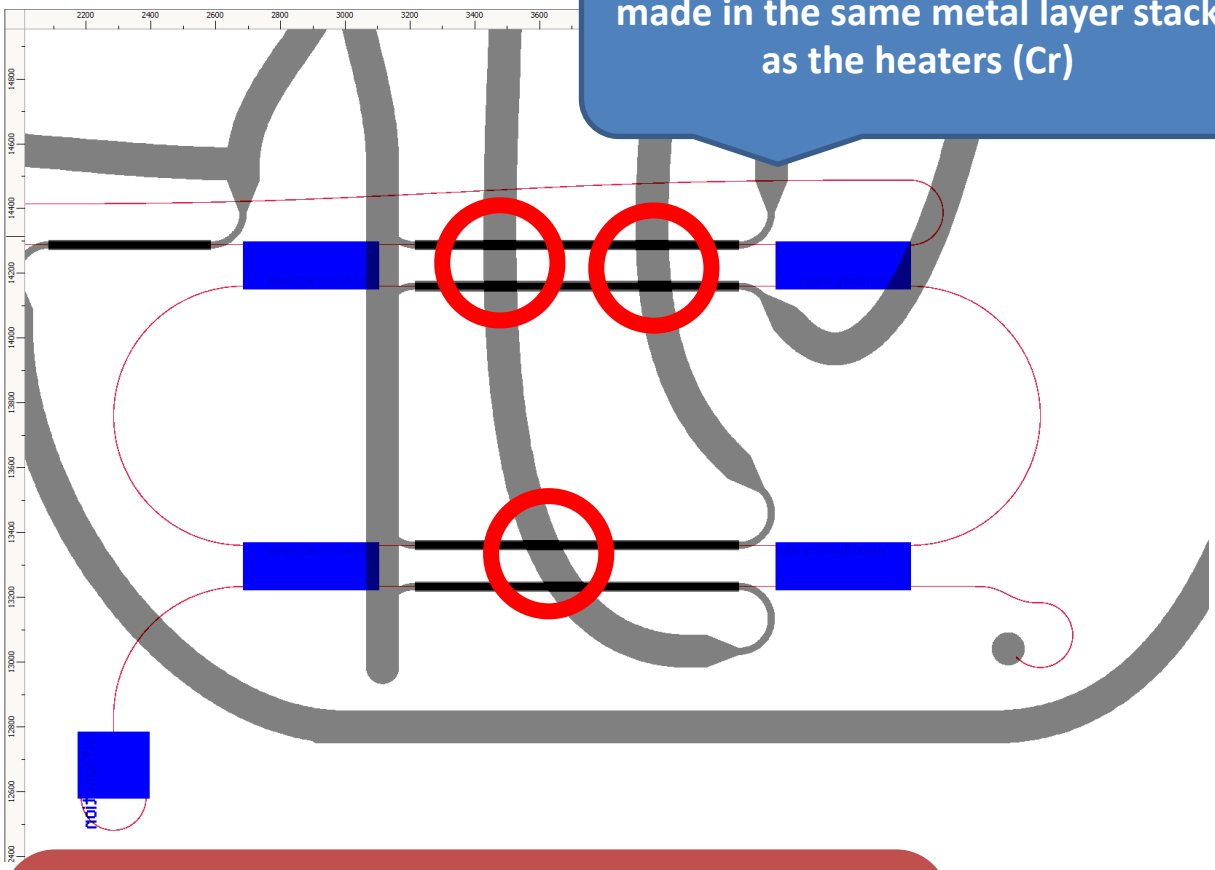
For the correct placement of the bondpads on the PIC, the d-parameter for each of the possible

Table 7: Distance of the first bondpad from the left facet.

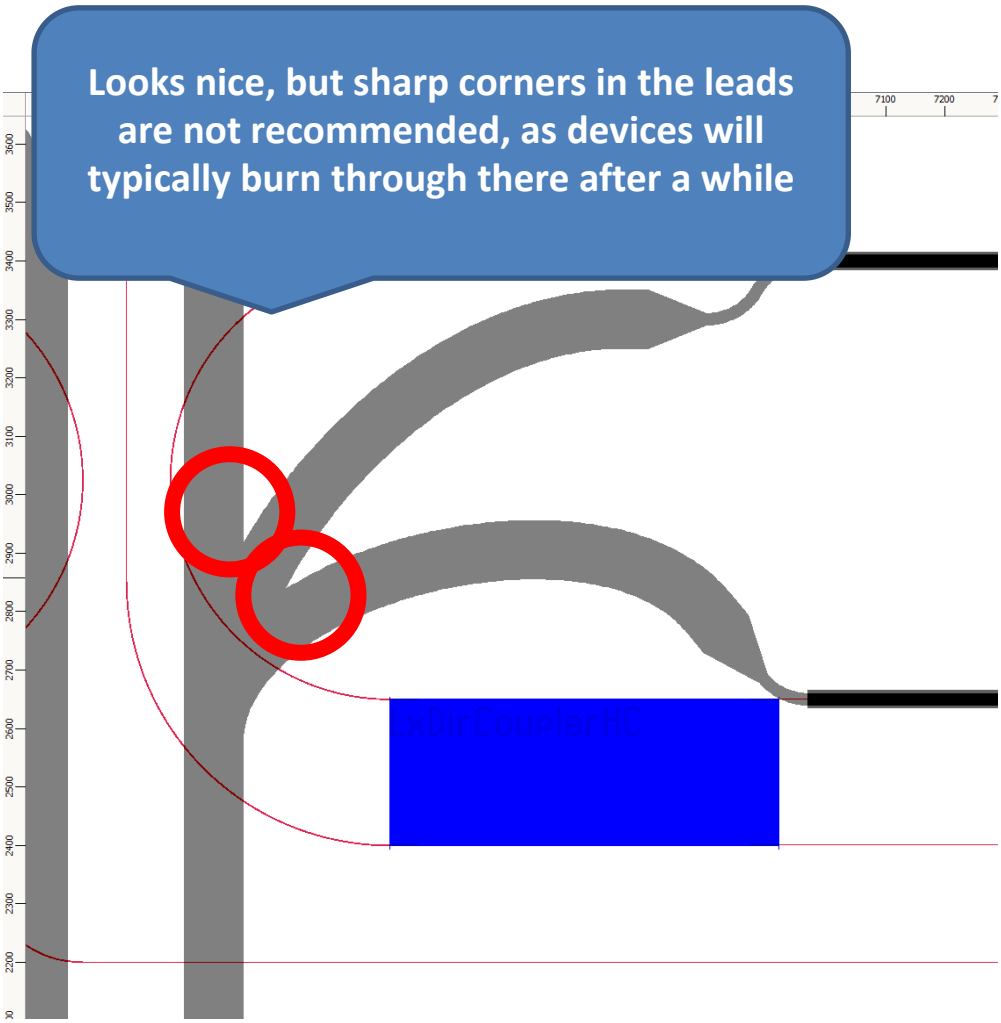
Chip size type #	d (µu)
#1	2825
#2	2825
#3	2825
#4	3325

4 Common Mistakes

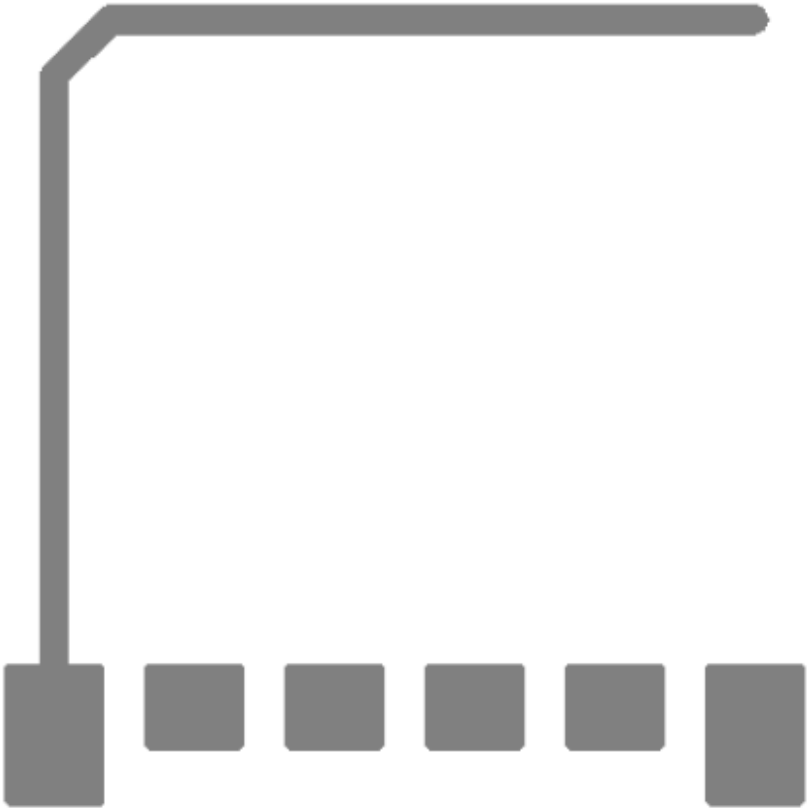
Leads to the heaters (Cr/Au) are made in the same metal layer stack as the heaters (Cr)



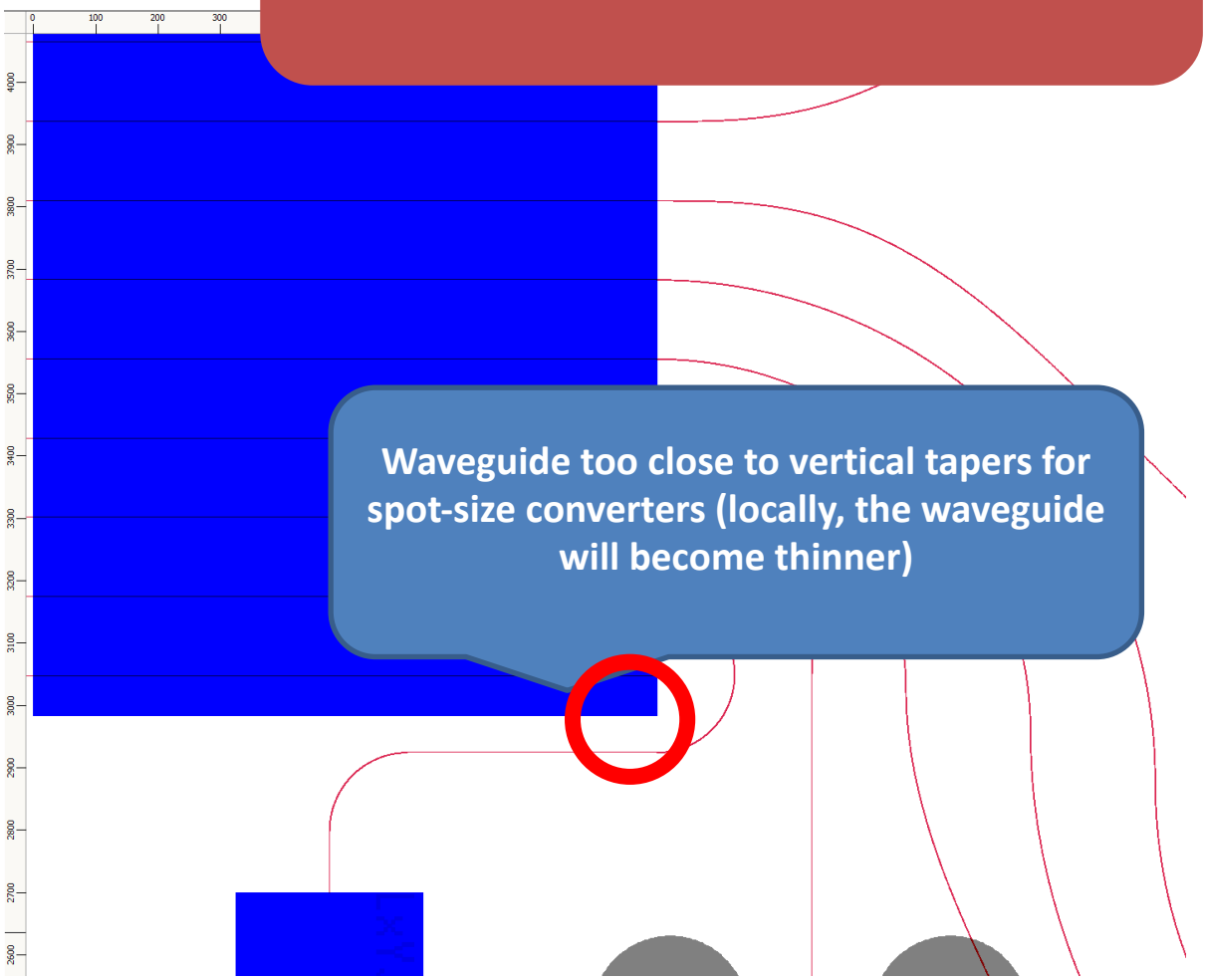
Therefore, leads are not allowed to cross heaters!

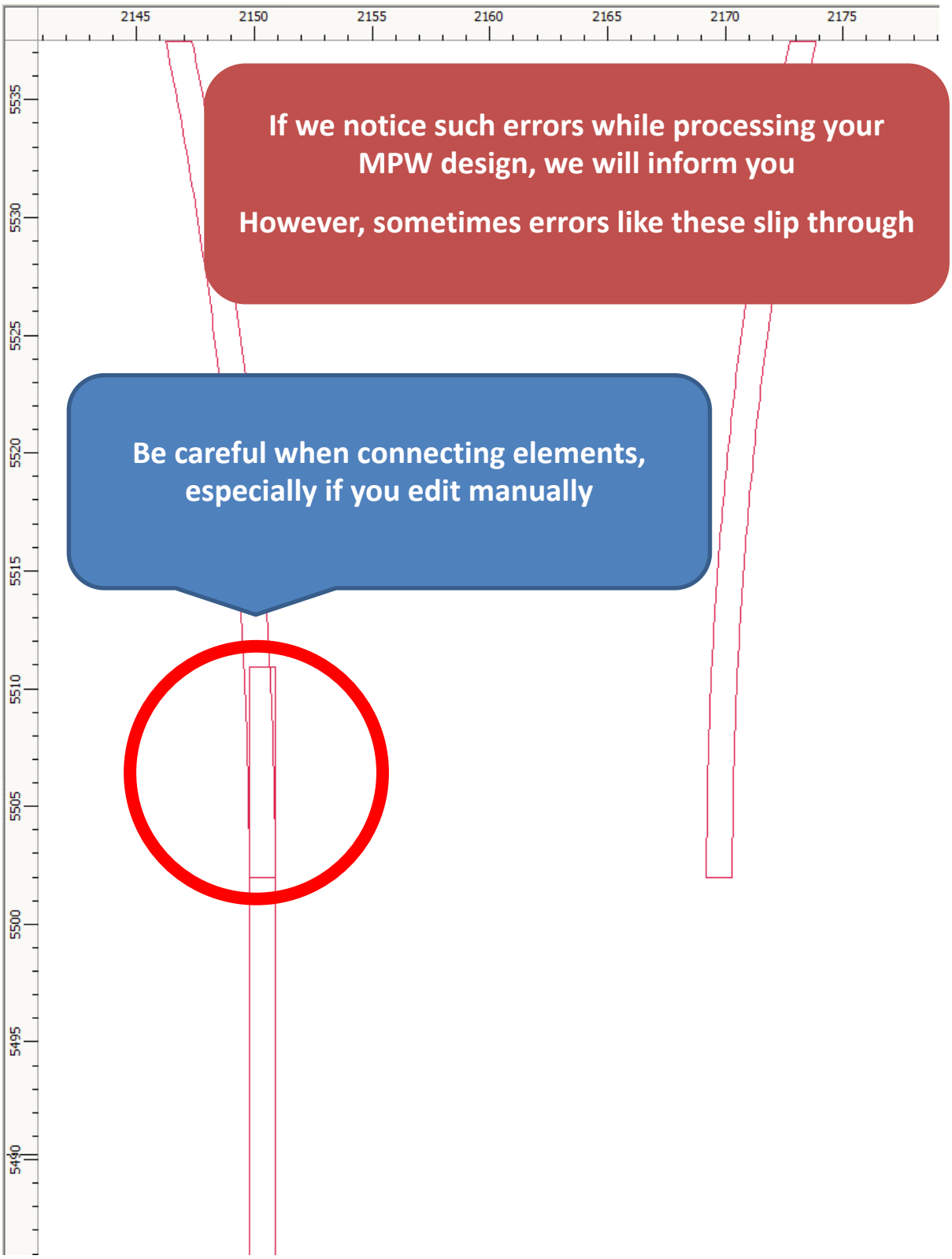

Looks nice, but sharp corners in the leads are not recommended, as devices will typically burn through there after a while

Therefore, we advise 135 degree angles



This has been solved by requiring more distance between components and LxSSC in the design rule check




2145
2150
2155
2160
2165
2170
2175
5535
5530
5525
5520
5515
5510
5505
5500
5495
5490
If we notice such errors while processing your MPW design, we will inform you
However, sometimes errors like these slip through
Be careful when connecting elements, especially if you edit manually